GSR811

Reset IC

Product Description

The GSR811 is microprocessor (μP) supervisory circuit used to monitor the power supplies in μP and digital systems. It provides excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5V, +3.3V, +3.0V, or 2.5V powered circuits. GSR811 also provide a debounced manual reset input.

The circuit perform a single function: it asserts a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. Reset thresholds suitable for operation with a variety of supply voltages are available.

The GSR811 has push-pull output and has an active-low $\overline{\text{RESET}}$ output. The reset comparator is designed to ignore fast transients on V_{CC}, and the output is guaranteed to be in the correct logic state for V_{CC} down to 1.2V within the range of the operating temperature .

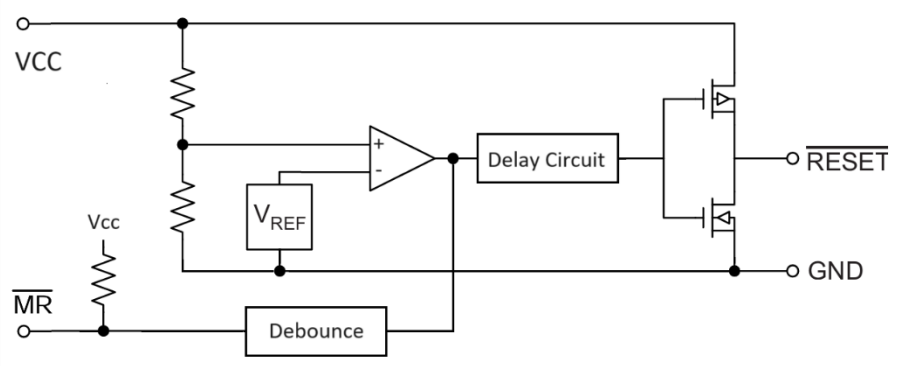
Features

- Manual Reset Available
- Precision monitoring of Supply Voltages
  – Available Threshold Options:
  - 4.63V (GSR811L)
  - 4.38V (GSR811M)
  - 4.00V (GSR811J)
  - 3.08V (GSR811T)
  - 2.93V (GSR811S)
  - 2.63V (GSR811R)
  - 2.32V (GSR811Z)
- 140ms Minimum Reset Pulse Width
- Push-Pull Configurations for $\overline{\text{RESET}}$ Output
- 10μA Supply Current Typically
- Power Supply Transient Immunity
- RoHS Compliant

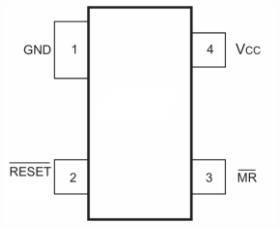
Applications

- Computers
- Controllers
- Intelligent Instruments
- Embedded Control Systems
- Battery-powered Equipment

Block Diagram



Packages & Pin Assignments

GSR811xKF (SOT-143)		
	**Pin No.**	**Name**
	1	**GND**
	2	**$\overline{\text{RESET}}$**
	3	**$\overline{\text{MR}}$**
	4	**Vcc**

Pin Description

Name	Type	Description
GND	-	Ground Pin.
$\overline{\text{RESET}}$	O	Active-Low Reset Output (Push-Pull). $\overline{\text{RESET}}$ Output remains low while VCC is below the reset threshold or while $\overline{\text{MR}}$ is held low, and for at least 140ms after the reset conditions are terminated.
$\overline{\text{MR}}$	I	Manual Reset Input. A logic low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted as long as $\overline{\text{MR}}$ is low and for 140ms after $\overline{\text{MR}}$ returns high. This active-low input has an internal 20kΩ pull-up resistor. It can be driven from a TTL or CMOS-logic line, or shorted to ground with a switch. Leave open if unused.
Vcc	I	Supply Voltage.

Ordering and Marking Information

GS P/N	Package	Marking	Reset Threshold
*GSR811LKF	SOT-143	AMAA	4.63V
*GSR811MKF	SOT-143	ANAA	4.38V
*GSR811JKF	SOT-143	AOAA	4.00V
GSR811TKF	SOT-143	APAA	3.08V
GSR811SKF	SOT-143	AQAA	2.93V
GSR811RKF	SOT-143	ARAA	2.63V
*GSR811ZKF	SOT-143	AZAZ	2.32V

★ Please contact a GS sales representative to inquire about production status.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.3 to +6.0	V
	All Other Inputs	-0.3 to V_{CC}+0.3	V
I_{OUT}	Output Current	20	mA
$T_{J(MAX)}$	Maximum Junction Temperature	150	ºC
T_{STG}	Storage Temperature Range	-65 to +150	ºC
$R_{\theta JA}$	Junction-to-ambient thermal resistance	300	°C/W
P_D	Power Dissipation	320	mW
T_{SOD}	Lead temperature (Soldering, 10 s)	300	ºC
V_{ESD}	Human-body model (HBM)	2000	V
	Charged-device model (CDM)	200	V

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Value	Unit
T_A	Operating Temperature Range	-40 to +85	ºC

Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted) (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Operating Voltage Range	T_A=0℃ ~ +70℃	1.0	-	5.5	V
		T_A=-40℃ ~ +85℃	1.2	-	5.5	
I_{CC}	Supply Current (T_A=-40℃ ~ +85℃)	V_{CC}=5.5V, GSR811(L/M/J)	-	10	25	μA
		V_{CC}=3.6V, GSR811(T/S/R/Z)	-	8	25	μA
V_{TH}	GSR811L Reset Threshold Voltage	T_A=25ºC	4.54	4.63	4.72	V
		T_A=-40 to 85ºC	4.50	-	4.75	
	GSR811M Reset Threshold Voltage	T_A=25ºC	4.29	4.38	4.47	V
		T_A=-40 to 85ºC	4.25	-	4.50	
	GSR811J Reset Threshold Voltage	T_A=25ºC	3.92	4.00	4.08	V
		T_A=-40 to 85ºC	3.89	-	4.10	

Electrical Characteristics (Continued)

V_{TH}	GSR811T Reset Threshold Voltage	T_A=25ºC	3.01	3.08	3.15	V
		T_A=-40 to 85ºC	3.00	-	3.17	
	GSR811S Reset Threshold Voltage	T_A=25ºC	2.86	2.93	3.00	V
		T_A=-40 to 85ºC	2.85	-	3.01	
	GSR811R Reset Threshold Voltage	T_A=25ºC	2.56	2.63	2.69	V
		T_A=-40 to 85ºC	2.55	-	2.70	
	GSR811Z Reset Threshold Voltage	T_A=25ºC	2.26	2.32	2.37	V
		T_A=-40 to 85ºC	2.25	-	2.38	
-	Reset Threshold Temp Coefficient			30		ppm/ºC
-	GSR811(L/M/J) V_{CC} to Reset Delay	V_{OD}=125mV		40		µs
	GSR811(T/S/R/Z) V_{CC} to Reset Delay	V_{OD}=125mV		20		
t_{RS}	Reset Active Timeout Period	T_A=-40 to 85ºC	140	240	560	ms
t_{MR}	$\overline{MR}$ Minimum Pulse Width		10			µs
	$\overline{MR}$ Glitch Immunity			100		ns
t_{MD}	$\overline{MR}$ to Reset Propagation Delay			0.5		µs
V_{IH}	GSR811(L/M/J)	V_{CC} > V_{TH} (max)	2.3			V
V_{IL}	$\overline{MR}$ Input Threshold				0.8	
V_{IH}	GSR811(L/M/J)	V_{CC} > V_{TH} (max)	0.8xV_{CC}			V
V_{IL}	$\overline{MR}$ Input Threshold				0.25xV_{CC}	
	$\overline{MR}$ Pull Up Resistance		10	20	30	kΩ
V_{OH}	GSR811(T/S/R/Z) Output High Voltage	V_{CC} > V_{TH} (max), I_{SOURCE} = 800µA	V_{CC}-1.5	-	-	V
	GSR811(T/S/R/Z) Output High Voltage	V_{CC} > V_{TH} (max), I_{SOURCE} = 500µA	0.8xV_{CC}	-	-	
V_{OL}	GSR811(L/M/J) Output Low Voltage	V_{CC} = V_{TH} (min), I_{SINK} = 3.2mA	-	-	0.4	V
	GSR811(T/S/R/Z) Output Low Voltage	V_{CC} = V_{TH} (min), I_{SOURCE} = 1.2mA	-	-	0.3	

Note 1: Production testing done at T_A = 25°C, over temperature limits specified by design only.

Application Information

Typical Application Circuit

The GSR811 is a supervisor circuit for microprocessor and digital systems.

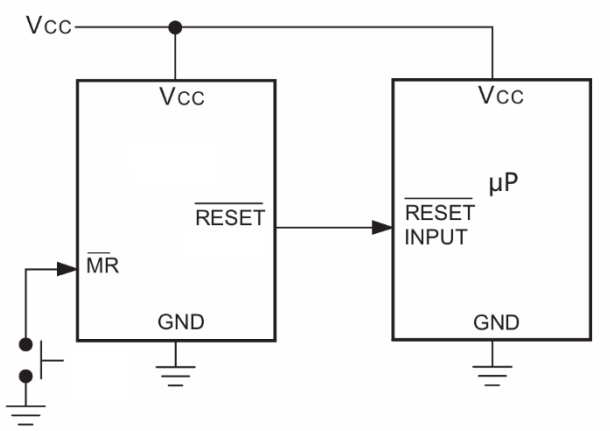


Figure. 1

Negative-Going Vcc Transients

GSR811 is relatively immune to short negative-going transients or glitches on Vcc. Figure 2 shows the maximum pulse width a negative-going Vcc transient can have without causing a reset pulse. In general, as the magnitude of the transient increases, going further below the threshold, the maximum allowable pulse width decreases. Typically, for the 4.63V and 4.38V version of the GSR811, a Vcc transient that goes 100 mV below the reset threshold and lasts 20 μs or less will not cause a reset pulse. A 0.1μF bypass capacitor mounted as close as possible to the Vcc pin will provide additional transient rejection.

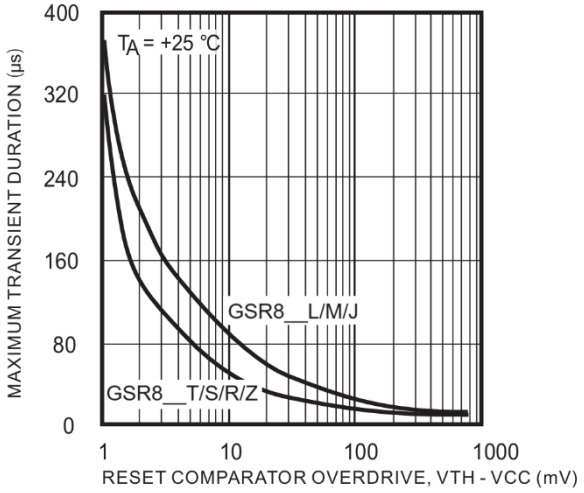


Figure. 2

Ensuring a Valid Reset Output Down to Vcc = 0 V

When Vcc falls below 1.2V, the GSR811 $\overline{\text{RESET}}$ output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to $\overline{\text{RESET}}$ can drift to undetermined voltages. This presents no problem in most applications since most μP and other circuitry is inoperative with Vcc below 1.2V.

However, in applications where $\overline{RESET}$ must be valid down to 0V, adding a pull-down resistor to $\overline{RESET}$ causes any stray leakage currents to flow to ground, holding $\overline{RESET}$ low (Figure 3).

R1's value is not critical; 100kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

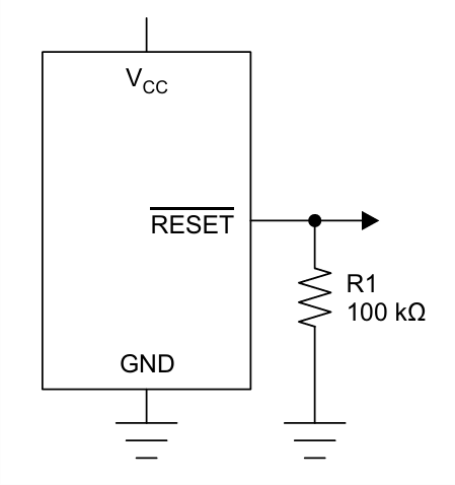


Figure. 3

Manual Reset Input

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for the Reset Active Timeout Period (t_{RS}) after $\overline{MR}$ returns high. This input has an internal 20kΩ pull-up resistor, so it can be left open if it is not used. $\overline{MR}$ can be driven with TTL or CMOS-logic levels, or with open drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1µF capacitor from $\overline{MR}$ to ground provides additional noise immunity.

Reference of Reset Curve

When Vcc supply voltage declines below the reset threshold, the active-low $\overline{RESET}$ output is Low.

When the Vcc supply voltage rises above the reset threshold, the active-low $\overline{RESET}$ output rises High after 240 ms typically.

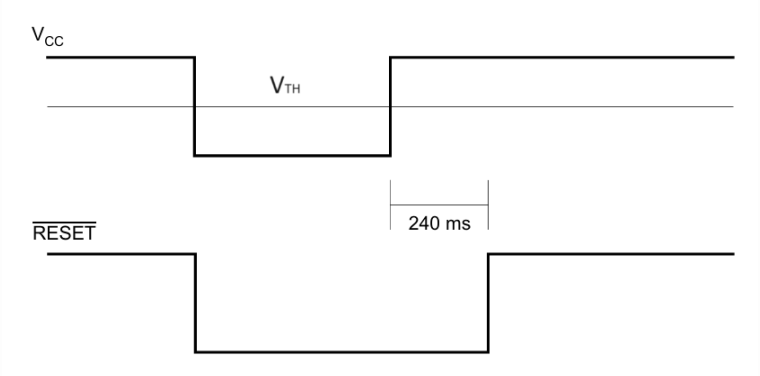
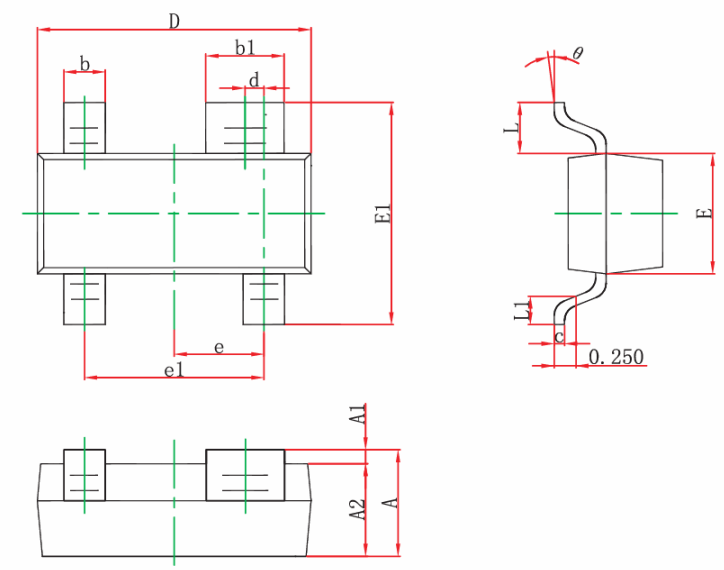


Figure. 4

Package Dimension

SOT-143



Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
b1	0.750	0.900	0.030	0.035
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
d	0.200 (TYP)		0.008 (TYP)	
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 (TYP)		0.037 (TYP)	
e1	1.800	2.000	0.071	0.079
L	0.550 (REF)		0.022 (REF)	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

NOTICE

Information furnished is believed to be accurate and reliable. However Globaltech Semiconductor assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Globaltech Semiconductor. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information without express written approval of Globaltech Semiconductor.

CONTACT US

GS Headquarter	
	4F.,No.43-1,Lane11,Sec.6,Minquan E.Rd Neihu District Taipei City 114, Taiwan (R.O.C)
	886-2-2657-9980
	886-2-2657-3630
@	sales_twn@gs-power.com

Wu-Xi Branch	
	No.21 Changjiang Rd., WND, Wuxi, Jiangsu, China (INFO. &. TECH. Science Park Building A 210 Room)
	86-510-85217051
	86-510-85211238
@	sales_cn@gs-power.com