

# GSMDS4906

## 40V N-Channel MOSFETs

### Product Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

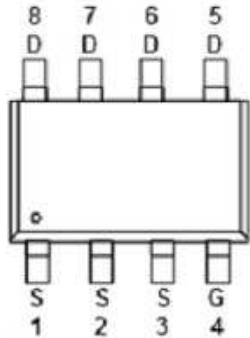
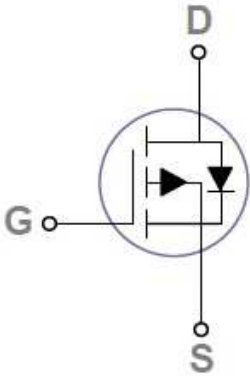
### Features

- 40V, 9A,  $R_{DS(ON)}=9m\Omega@V_{GS}=-10V$
- Improved dv/dt capability
- Fast switching
- Green Device Available
- SOP-8 package design

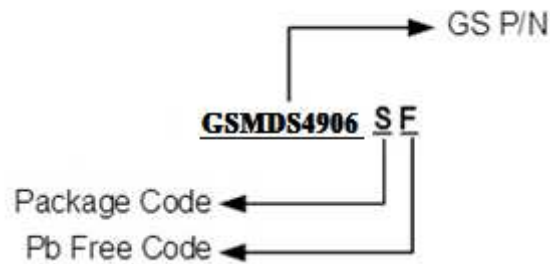
### Applications

- Notebook
- Load Switch
- LED applications
- Hand-Held Device

### Packages & Pin Assignments

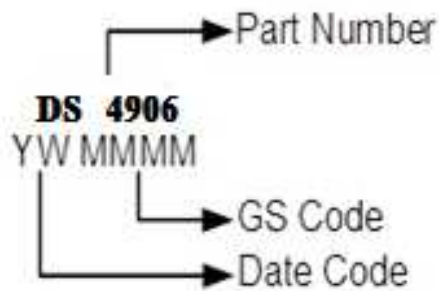
GSMDS4906SF(SOP-8)			
			
			
Pin	Description	Pin	Description
1	Source	5	Drain
2	Source	6	Drain
3	Source	7	Drain
4	Gate	8	Drain

## Ordering Information



Part Number	Package	Quantity/Reel
GSMDS4906SF	SOP-8	4000 PCS

## Marking Information



## Absolute Maximum Ratings

$T_A=25^{\circ}\text{C}$  Unless otherwise noted

Symbol	Parameter	Typical	Unit
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_A=25^{\circ}\text{C}$	9
		$T_A=100^{\circ}\text{C}$	5.7
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	36	A
$P_D$	Power Dissipation ( $T_A=25^{\circ}\text{C}$ )	1.47	W
	Power Dissipation (Derate above $25^{\circ}\text{C}$ )	0.012	W/ $^{\circ}\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to +150	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to +150	$^{\circ}\text{C}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	62.5	$^{\circ}\text{C}/\text{W}$

## Electrical Characteristics

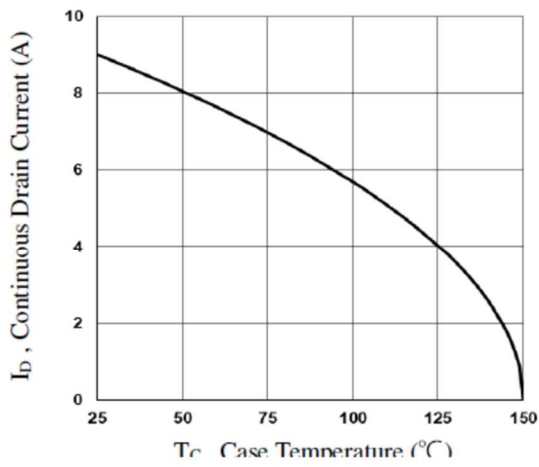
T<sub>J</sub>=25°C Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	40			V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA		0.03		V/°C
V <sub>GS(th)</sub>	Gate Threshold Voltage		1.2	1.8	2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA		5		mV/°C
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V			1	uA
		V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =85°C			10	
I <sub>S</sub>	Continuous Source Current	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current			15	A
I <sub>SM</sub>	Pulsed Source Current				30	
R <sub>DS(on)</sub>	Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =8A		7	9	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =4A		9.5	13	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-10V, I <sub>D</sub> =10A		13		S
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =1A			1	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, dI/dt=100A/μs		17		nS
Q <sub>rr</sub>	Reverse Recovery Charge			2.8		nC
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, F=1MHz		2.2		Ω
<b>Dynamic</b>						
Q <sub>g</sub>	Total Gate Charge <sup>2,3</sup>	V <sub>DS</sub> =20V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A		12.2	24	nC
Q <sub>gs</sub>	Gate-Source Charge <sup>2,3</sup>			3.3	7	
Q <sub>gd</sub>	Gate-Drain Charge <sup>2,3</sup>			6.7	13	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, F=1MHz		1220	2200	pF
C <sub>oss</sub>	Output Capacitance			130	250	
C <sub>rss</sub>	Reverse Transfer Capacitance			55	110	
t <sub>d(on)</sub>	Turn-On Time <sup>2,3</sup>	V <sub>DD</sub> =15V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V, R <sub>G</sub> =2.2Ω		13.2	25	ns
t <sub>r</sub>				2.2	5	
t <sub>d(off)</sub>	Turn-Off Time <sup>2,3</sup>			72	130	
t <sub>f</sub>				4.5	10	

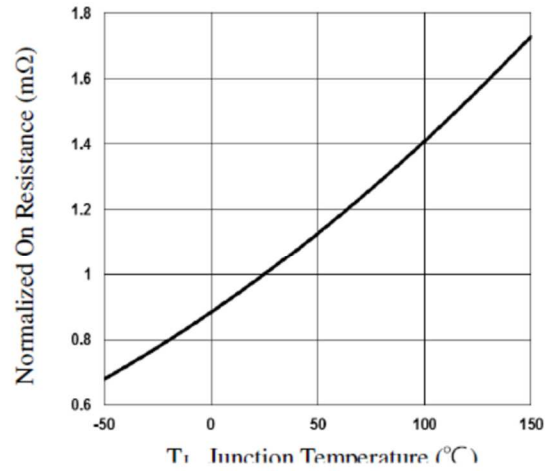
Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
3. Essentially independent of operating temperature.

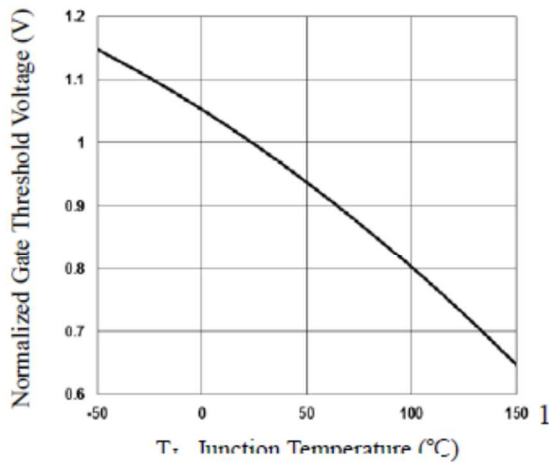
## Typical Performance Characteristics



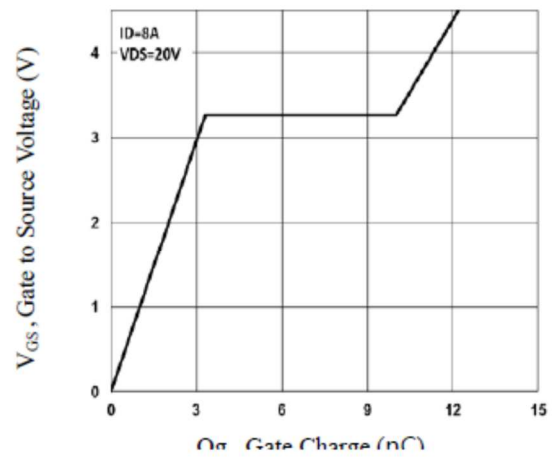
**Fig.1 Continuous Drain Current vs.  $T_C$**



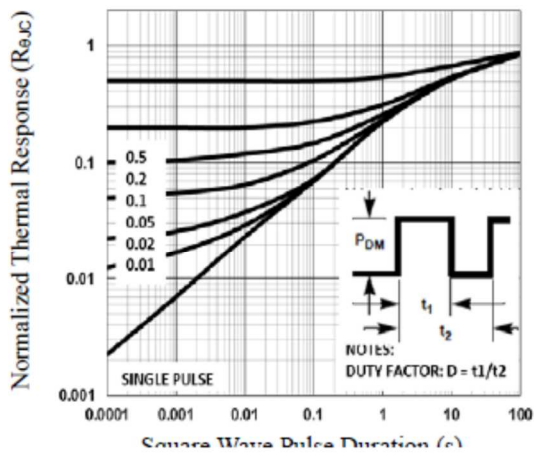
**Fig.2 Normalized  $R_{DS(on)}$  vs.  $T_J$**



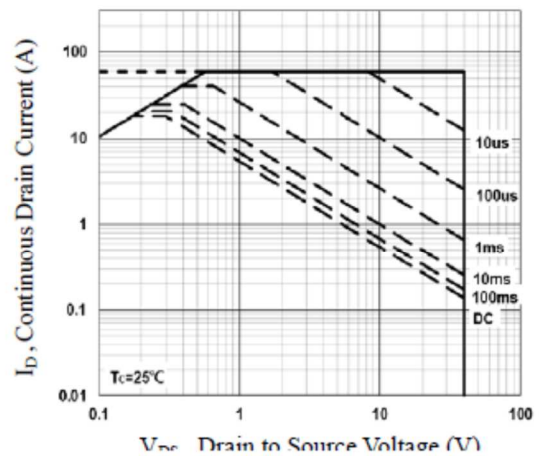
**Fig.3 Normalized  $V_{th}$  vs.  $T_J$**



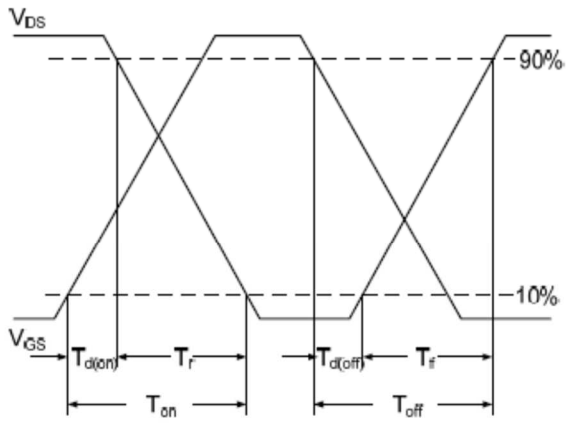
**Fig.4 Gate Charge Waveform**



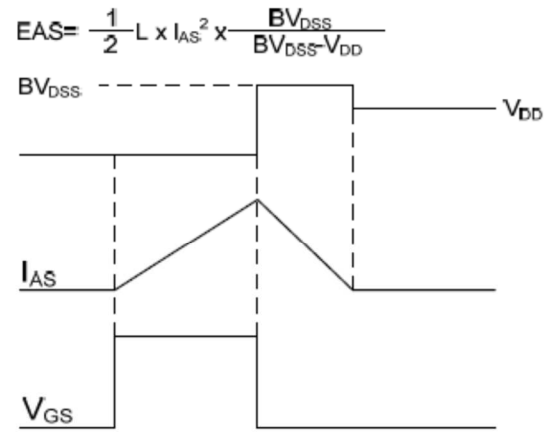
**Fig.5 Normalized Transient Impedance**



**Fig.6 Maximum Safe Operation Area**



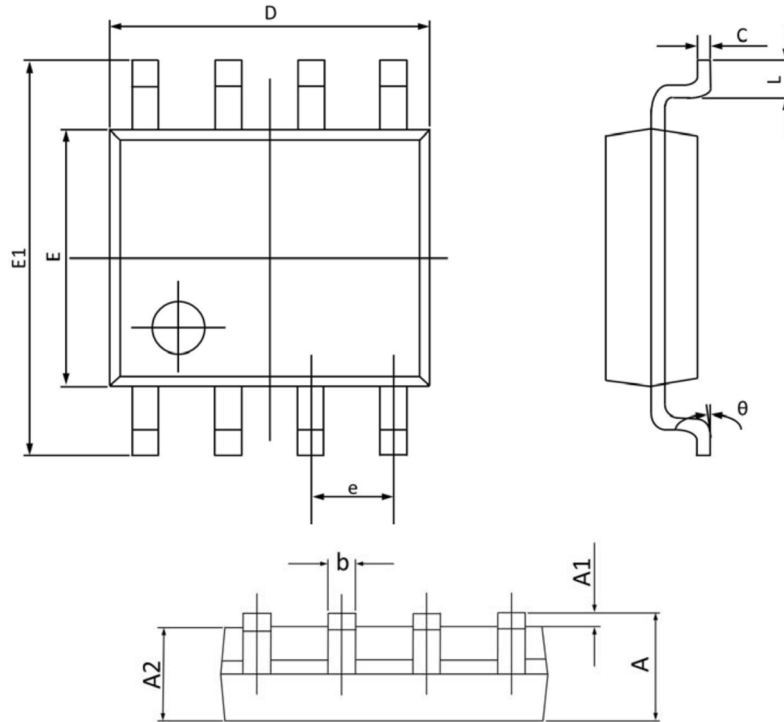
**Fig.7 Switching Time Waveform**



**Fig.8 EAS Waveform**

Package Dimension

## SOP-8 PACKAGE









Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MAX	MIN	MAX	MIN
A	1.750	1.350	0.069	0.053
A1	0.250	0.100	0.010	0.004
A2	1.500	1.300	0.059	0.051
b	0.490	0.350	0.019	0.014
C	0.260	0.190	0.010	0.007
D	5.100	4.700	0.201	0.185
E	4.100	3.700	0.161	0.146
E1	6.200	5.800	0.244	0.228
e	1.27BSC		0.05BSC	
L	0.900	0.400	0.035	0.016
theta	8°	0°	8°	0°

## NOTICE

Information furnished is believed to be accurate and reliable. However Globaltech Semiconductor assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Globaltech Semiconductor. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information without express written approval of Globaltech Semiconductor.

## CONTACT US

GS Headquarter	
	4F.,No.43-1,Lane11,Sec.6,MinquanE.RdNeihuDistrictTaipeiCity 114, Taiwan (R.O.C)
	886-2-2657-9980
	886-2-2657-3630
	sales_twn@gs-power.com

RD Division	
	824 Bolton DriveMilpitas. CA. 95035
	1-408-457-0587