

GSMDD6966A

60V N-Channel MOSFETs

Product Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

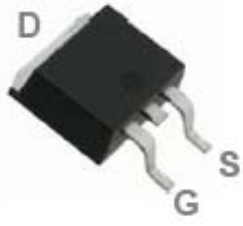
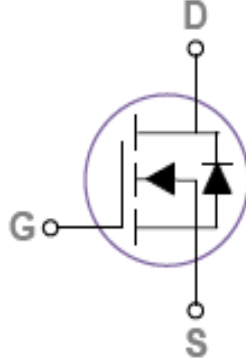
Features

- 60V, 55A, $R_{DS(ON)}=8.2m\Omega@V_{GS}=10V$
- Improved dv/dt capability
- Fast switching
- Green Device Available
- TO-252-2L package design

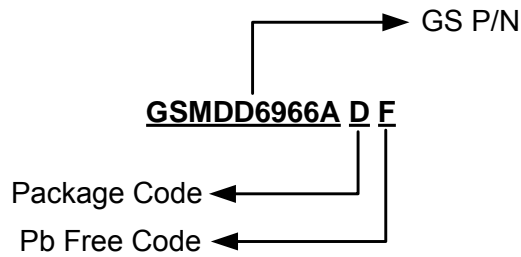
Applications

- Networking
- Load Switch
- LED Applications

Packages & Pin Assignments

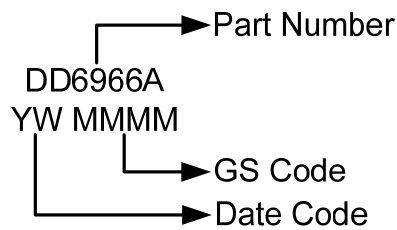
GSMDD6966ADF (TO-252-2L)	
 <p>Top View</p>	
Description	
Gate	
Source	
Drain	

Ordering Information



Part Number	Package	Quantity Reel
GSMDD6966ADF	TO-252-2L	2500 PCS

Marking Information



Absolute Maximum Ratings

$T_C=25^\circ\text{C}$ Unless otherwise noted

Symbol	Parameter	Typical	Unit
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 25	V
I_D	Continuous Drain Current	$T_C=25^\circ\text{C}$	55
		$T_C=100^\circ\text{C}$	34.8
I_{DM}	Pulsed Drain Current (Note 1)	220	A
EAS	Single Pulse Avalanche Energy (Note 2)	238	mJ
IAS	Single Pulse Avalanche Current (Note 2)	69	A
P_D	Power Dissipation ($T_C=25^\circ\text{C}$)	102	W
	Power Dissipation (Derate above 25°C)	0.82	W/ $^\circ\text{C}$
T_J	Operating Junction Temperature Range	-50 to +150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-50 to +150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	62	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance-Junction to Case	1.22	$^\circ\text{C}/\text{W}$

Note 1: Repetitive Rating: Pulsed width limited by maximum junction temperature.

Note 2: $V_{DD}=25\text{V}$, $V_{GS}=10\text{V}$, $L=0.1\text{mH}$, $I_{AS}=69\text{A}$, Starting $T_J=25^\circ\text{C}$.

Electrical Characteristics

$T_J=25^\circ\text{C}$ Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60			V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$		0.05		$V/^\circ\text{C}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient			-5		$\text{mV}/^\circ\text{C}$
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 25V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=60V, V_{GS}=0V$			1	μA
		$V_{DS}=48V, V_{GS}=0V$, $T_J=125^\circ\text{C}$			10	
I_S	Continuous Source Current	$V_G=V_D=0V$, Force Current			55	A
I_{SM}	Pulsed Source Current				110	
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=10V, I_D=20A$		6.8	8.2	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=10V, I_D=3A$		10		S
V_{SD}	Diode Forward Voltage	$V_{GS}=0V, I_S=1A$			1	V
Dynamic						
Q_g	Total Gate Charge (Note 3,4)	$V_{DS}=30V, V_{GS}=10V$, $I_D=10A$		26.9	48	nC
Q_{gs}	Gate-Source Charge (Note 3,4)			10.7	20	
Q_{gd}	Gate-Drain Charge (Note 3,4)			6.55	13	
C_{iss}	Input Capacitance	$V_{DS}=30V, V_{GS}=0V$, $f=1\text{MHz}$		1690	2600	pF
C_{oss}	Output Capacitance			294	450	
C_{rss}	Reverse Transfer Capacitance			90	180	
$t_{d(on)}$	Turn-On Time (Note 3,4)	$V_{DD}=30V, I_D=1A$, $V_{GS}=10V, R_G=6\Omega$		16	30	ns
t_r				12	24	
$t_{d(off)}$	Turn-Off Time (Note 3,4)			32	55	
t_f				23	40	
R_g	Gate Resistance		$V_{DS}=0V, V_{GS}=0V$, $f=1\text{MHz}$		1.3	

Note 3: The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

Note 4: Essentially independent of operating temperature.

Typical Performance Characteristics

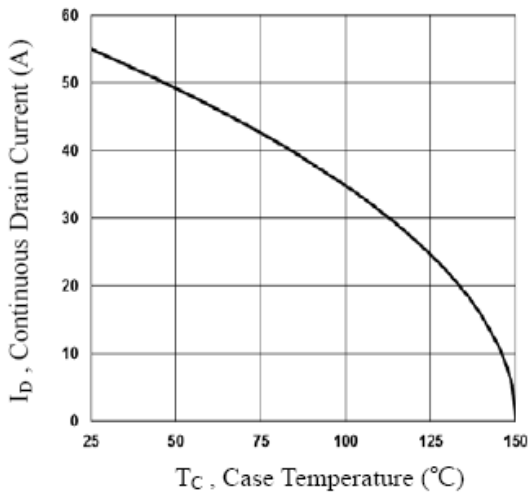


Fig.1 Continuous Drain Current vs. T_C

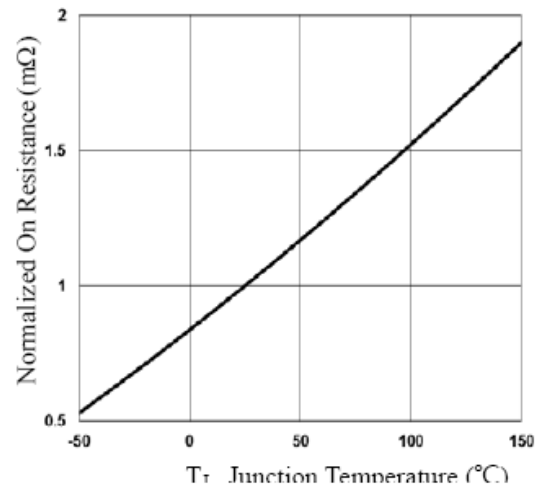


Fig.2 Normalized $R_{DS(on)}$ vs. T_J

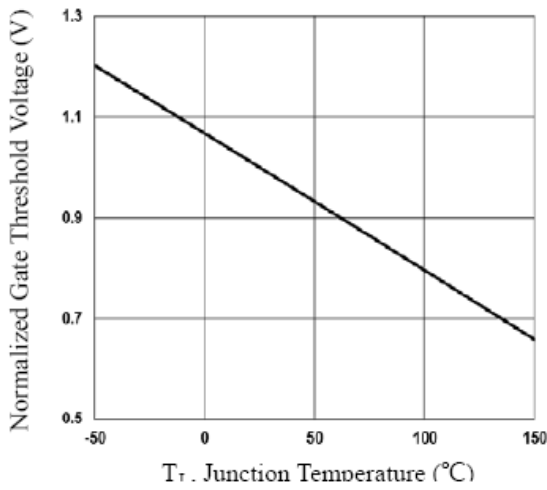


Fig.3 Normalized V_{th} vs. T_J

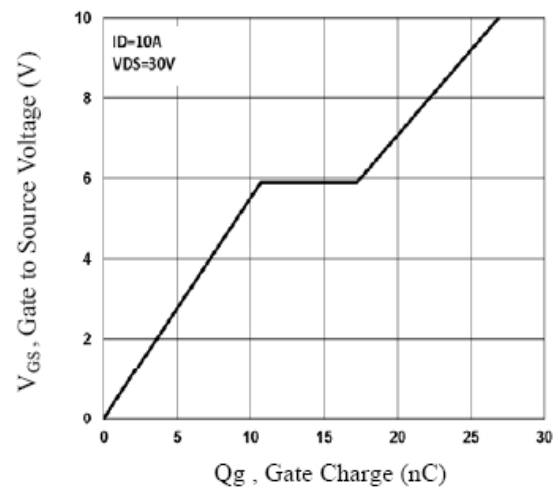


Fig.4 Gate Charge Characteristics

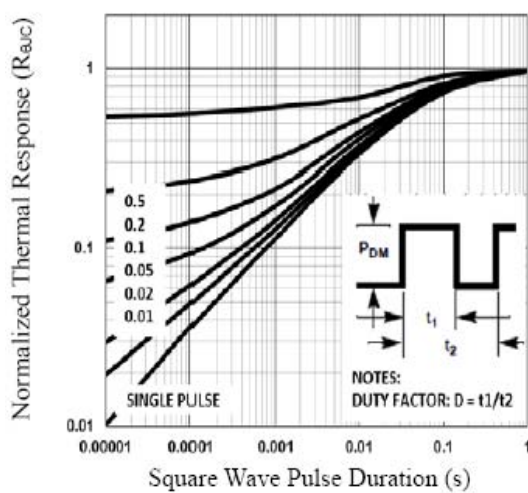


Fig.5 Normalized Transient Impedance

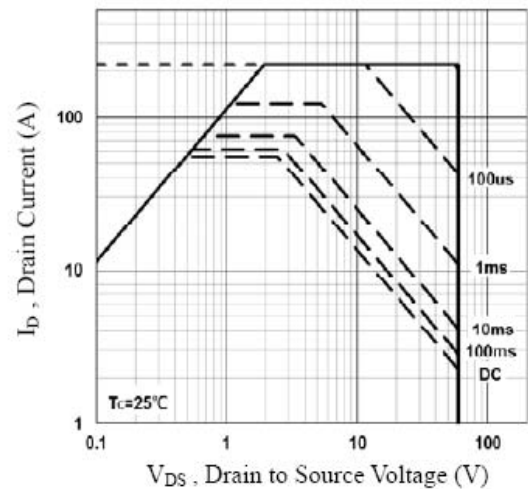
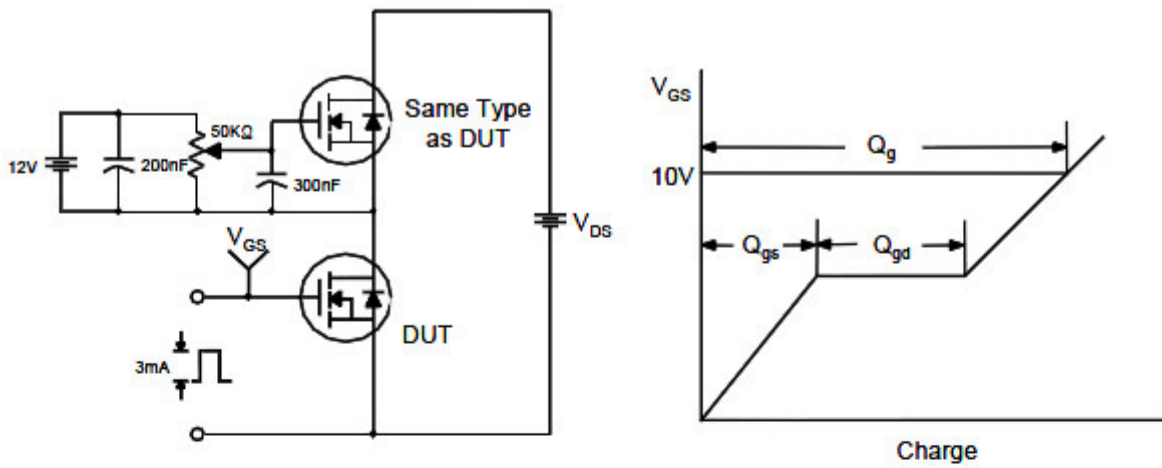


Fig.6 Maximum Safe Operation Area

Typical Performance Characteristics (Continue)

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

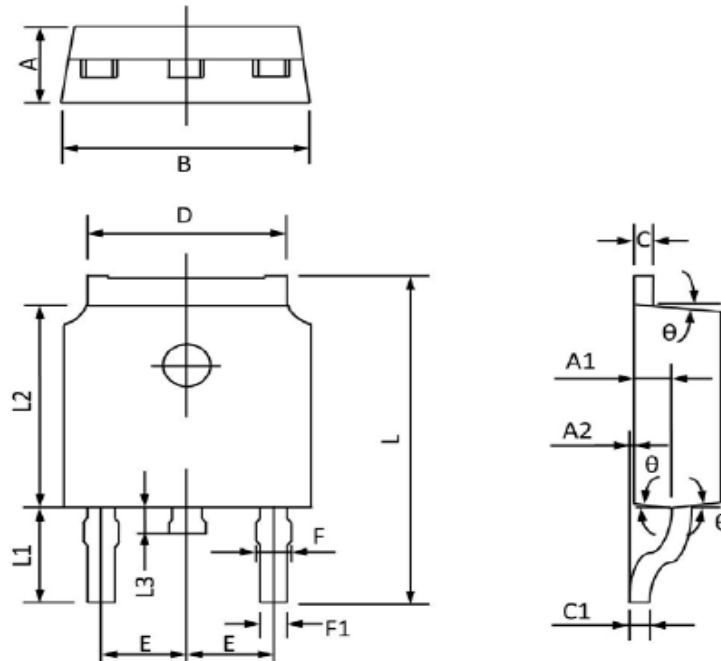


Unclamped Inductive Switching Test Circuit & Waveforms



Package Dimension

TO-252-2L










Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.20	2.40	0.087	0.094
A1	0.91	1.11	0.036	0.044
A2	0.00	0.15	0.000	0.006
B	6.40	6.80	0.252	0.268
C	0.46	0.58	0.018	0.023
C1	0.46	0.58	0.018	0.023
D	5.10	5.50	0.201	0.217
E	2.186	2.386	0.086	0.094
F	0.60	0.94	0.024	0.037
F1	0.50	0.86	0.020	0.034
L	9.40	10.40	0.370	0.409
L1	2.40	3.00	0.094	0.118
L2	5.40	6.20	0.213	0.244
L3	0.60	1.20	0.024	0.047
θ	3°	9°	3°	9°



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