

# GSMDD4963

## 40V P-Channel MOSFETs

### Product Description

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

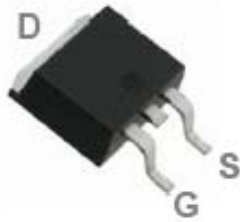
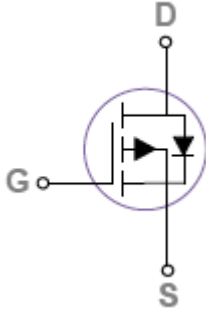
### Features

- -40V, -45A,  $R_{DS(ON)}=17m\Omega@V_{GS}=10V$
- Improved dv/dt capability
- Fast switching
- Green Device Available
- TO-252-2L package design

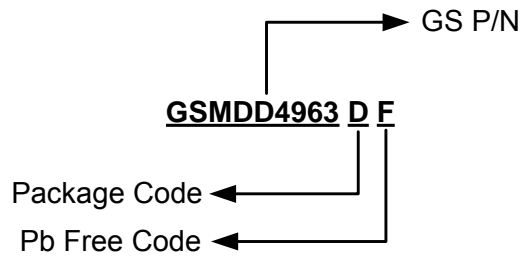
### Applications

- Motor Drive
- POL Applications
- LED Lighting

### Packages & Pin Assignments

GSMDD4963DF (TO-252-2L)	
 <p>Top View</p>	
<b>Description</b>	
Gate	
Source	
Drain	

## Ordering Information



Part Number	Package	Quantity Reel
GSMDD4963DF	TO-252-2L	2500 PCS

## Absolute Maximum Ratings

$T_C=25^{\circ}\text{C}$  Unless otherwise noted

Symbol	Parameter	Typical	Unit
$V_{DS}$	Drain-Source Voltage	-40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_A=25^{\circ}\text{C}$	-45
		$T_C=100^{\circ}\text{C}$	-28
$I_{DM}$	Pulsed Drain Current (Note 1)	-180	A
EAS	Single Pulse Avalanche Energy (Note 2)	100	mJ
IAS	Single Pulse Avalanche Current (Note 2)	-45	A
$P_D$	Power Dissipation ( $T_C=25^{\circ}\text{C}$ )	62.5	W
	Power Dissipation (Derate above $25^{\circ}\text{C}$ )	0.5	W/ $^{\circ}\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to +150	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to +150	$^{\circ}\text{C}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	62	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance-Junction to Case	2	$^{\circ}\text{C}/\text{W}$

Note 1: Repetitive Rating: Pulsed width limited by maximum junction temperature.

Note 2:  $V_{DD}=-25\text{V}$ ,  $V_{GS}=-10\text{V}$ ,  $L=0.1\text{mH}$ ,  $I_{AS}=-45\text{A}$ , Starting  $T_J=25^{\circ}\text{C}$ .

## Electrical Characteristics

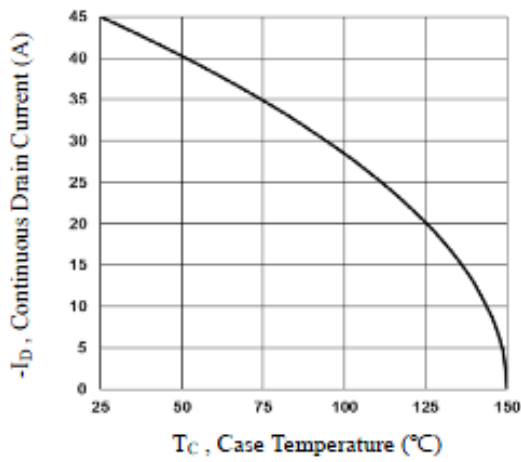
$T_J=25^{\circ}\text{C}$  Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	-40			V
$\Delta BV_{DSS}/\Delta T_J$	$BV_{DSS}$ Temperature Coefficient	Reference to $25^{\circ}\text{C}$ , $I_D=-1\text{mA}$		-0.05		$V/^{\circ}\text{C}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.2	-1.6	-2.5	V
$I_{GSS}$	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-40V, V_{GS}=0V$ $T_J=25^{\circ}\text{C}$			1	uA
		$V_{DS}=-32V, V_{GS}=0V$ , $T_J=125^{\circ}\text{C}$			10	
$I_S$	Continuous Source Current	$V_G=V_D=0V$ , Force Current			-45	A
$I_{SM}$	Pulsed Source Current (Note 3)				-90	
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=-10V, I_D=-15A$		15	17	m $\Omega$
		$V_{GS}=-4.5V, I_D=-10A$		22	25	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=-10V, I_D=-3A$		13		S
$V_{SD}$	Diode Forward Voltage (Note 3)	$V_{GS}=0V, I_S=-1A$			-1	V
<b>Dynamic</b>						
$Q_g$	Total Gate Charge (Note 3,4)	$V_{DS}=-20V, V_{GS}=-4.5V$ , $I_D=5A$		19	38	nC
$Q_{gs}$	Gate-Source Charge (Note 3,4)			6.2	12	
$Q_{gd}$	Gate-Drain Charge (Note 3,4)			5.2	10	
$C_{iss}$	Input Capacitance	$V_{DS}=-25V, V_{GS}=0V$ , $f=1\text{MHz}$		2260	3300	pF
$C_{oss}$	Output Capacitance			170	250	
$C_{rss}$	Reverse Transfer Capacitance			130	190	
$t_{d(on)}$	Turn-On Time (Note 3,4)	$V_{DD}=-20V, I_D=-1A$ , $V_{GS}=-10V, R_G=6\Omega$		18.2	36	ns
$t_r$				4.2	8.5	
$t_{d(off)}$	Turn-Off Time (Note 3,4)			72	140	
$t_f$				9.8	20	
$R_g$	Gate Resistance		$V_{DS}=0V, V_{GS}=0V$ , $f=1\text{MHz}$		7.5	

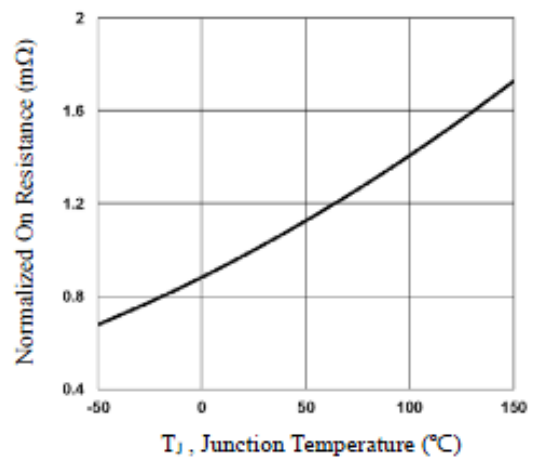
Note 3: The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .

Note 4: Essentially independent of operating temperature.

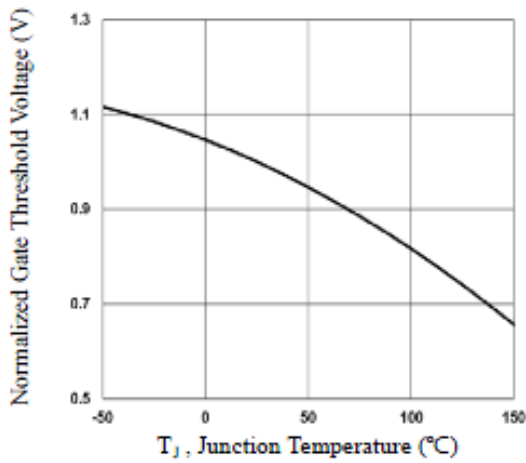
## Typical Performance Characteristics



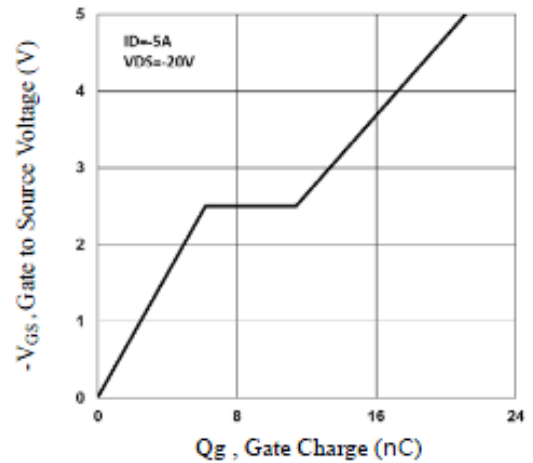
**Fig.1 Continuous Drain Current vs.  $T_c$**



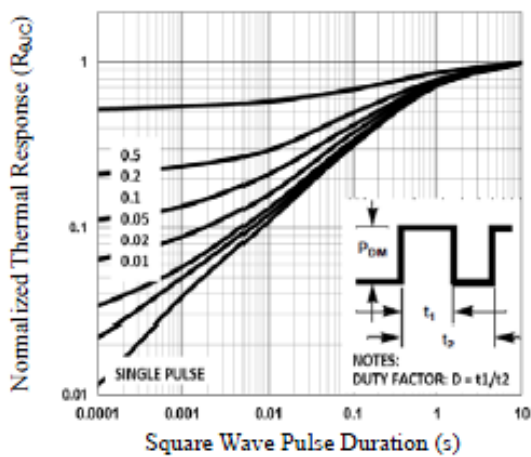
**Fig.2 Normalized  $R_{DS(on)}$  vs.  $T_j$**



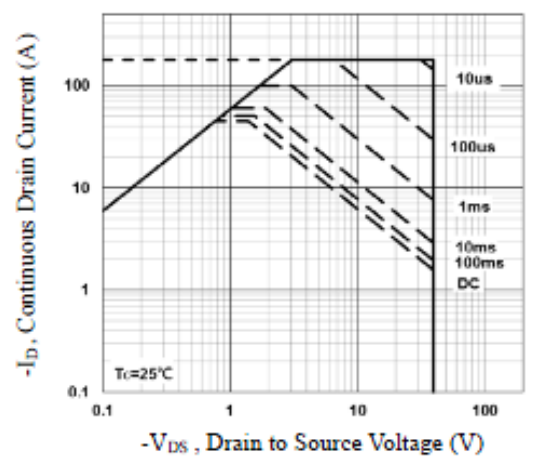
**Fig.3 Normalized  $V_{th}$  vs.  $T_j$**



**Fig.4 Gate Charge Waveform**



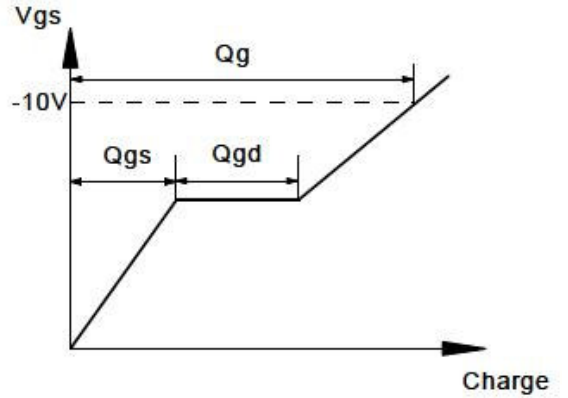
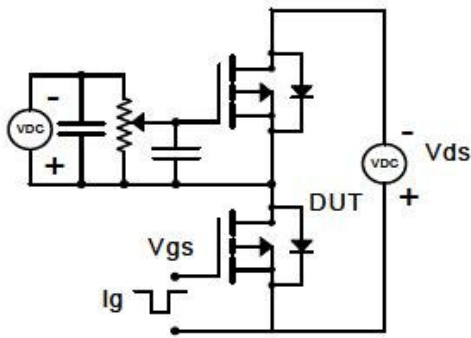
**Fig.5 Normalized Transient Impedance**



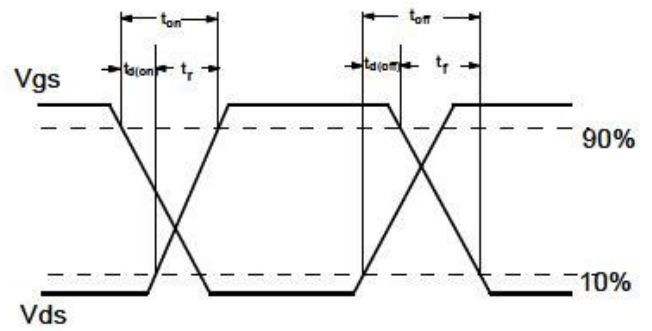
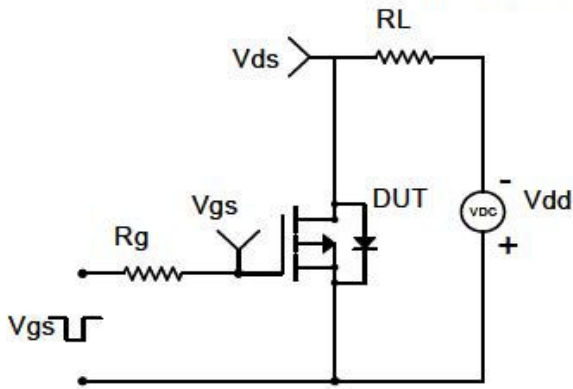
**Fig.6 Maximum Safe Operation Area**

## Typical Performance Characteristics (Continue)

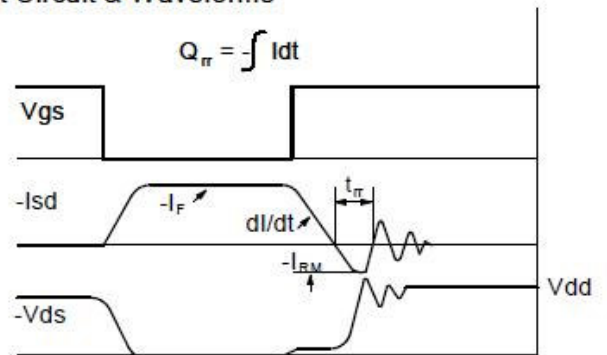
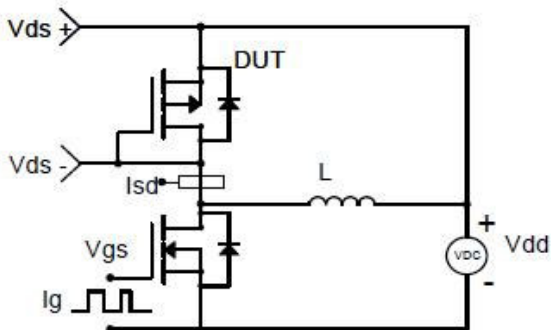
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms

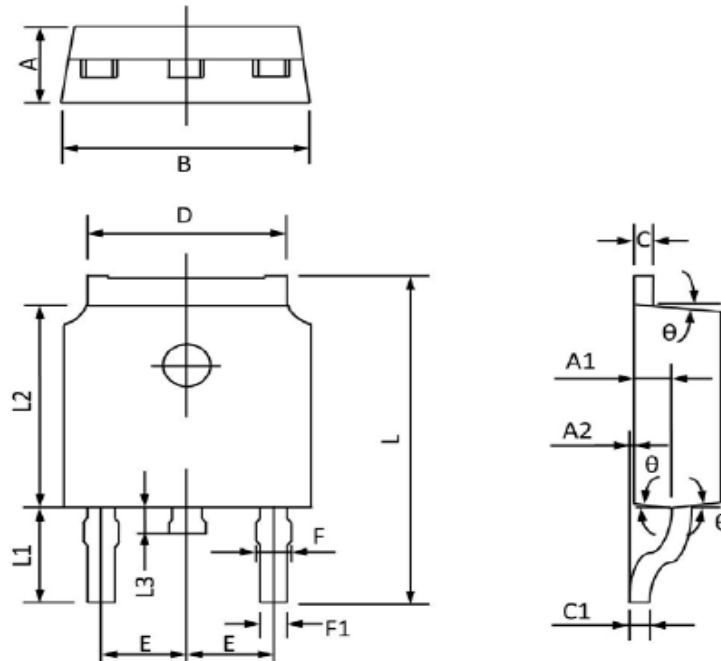


### Diode Recovery Test Circuit & Waveforms

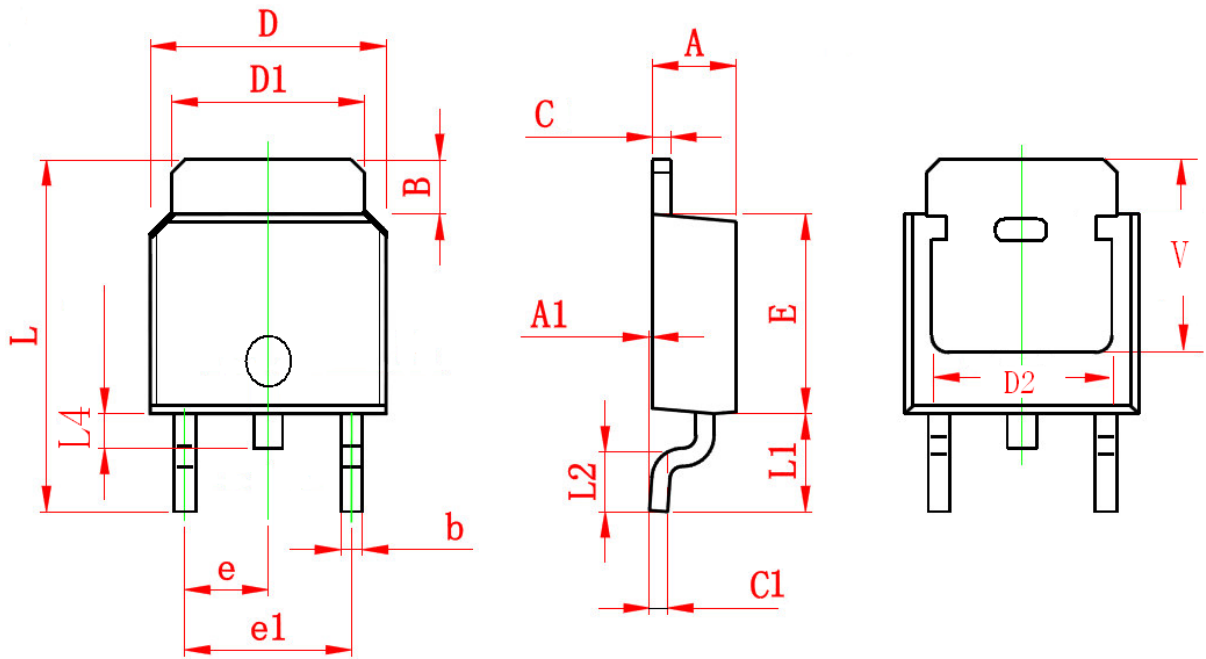


## Package Dimension

### TO-252-2L



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.20	2.40	0.087	0.094
A1	0.91	1.11	0.036	0.044
A2	0.00	0.15	0.000	0.006
B	6.50	6.70	0.256	0.264
C	0.46	0.58	0.018	0.030
C1	0.46	0.58	0.018	0.030
D	5.10	5.46	0.201	0.215
E	2.186	2.386	0.086	0.094
F	0.74	0.94	0.029	0.037
F1	0.66	0.86	0.026	0.034
L	9.80	10.40	0.386	0.409
L1	2.9 (REF)		0.114 (REF)	
L2	6.00	6.20	0.236	0.244
L3	0.60	1.00	0.024	0.039
$\theta$	3°	9°	3°	9°







### Dimensions



SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	2.200	2.400	0.087	0.094
A1	0.000	0.13	0.000	0.0051
B	0.89	1.27	0.035	0.05
b	0.64	0.88	0.0252	0.0346
C	0.430	0.58	0.017	0.023
C1	0.430	0.60	0.017	0.0236
D	6.350	6.730	0.250	0.265
D1	5.200	5.460	0.205	0.215
E	6.000	6.220	0.236	0.244
e	2.300 TYP		0.091 TYP	
e1	4.500	4.700	0.177	0.185
L	9.400	10.400	0.37	0.409
L1	2.743 REF		0.108 REF	
L2	1.400	1.780	0.055	0.070
L4	0.600	1.01	0.024	0.0398
V	5.350 REF		0.211 REF	
D2	4.830 REF		0.190 REF	

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