

# GSMDC3904Z

## 30V N-Channel MOSFETs

### Product Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

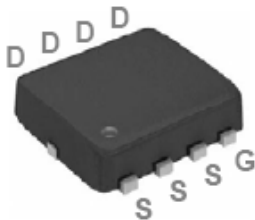
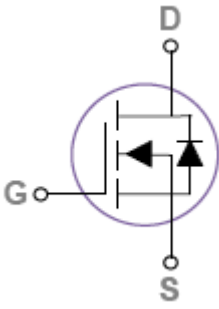
### Features

- 30V, 80A,  $R_{DS(ON)}=3.8m\Omega@V_{GS}=10V$
- Improved dv/dt capability
- Fast switching
- 100% EAS guaranteed
- Green Device Available
- DFN3X3-8L package design

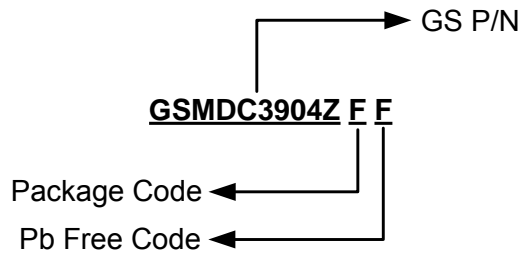
### Applications

- MB / VGA / Vcore
- POL Applications
- SMPS 2nd SR

### Packages & Pin Assignments

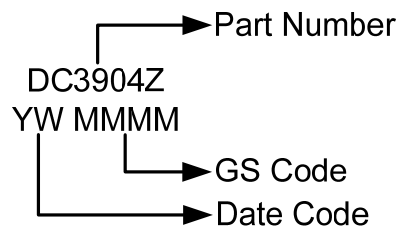
GSMDC3904ZFF (DFN3X3-8L)	
 <p>Top View</p>	
	
Pin	Description
1	Source
2	Source
3	Source
4	Gate
5	Drain
6	Drain
7	Drain
8	Drain

## Ordering Information



Part Number	Package
GSMDC3904ZFF	DFN3X3-8L

## Marking Information



## Absolute Maximum Ratings

T<sub>A</sub>=25°C Unless otherwise noted

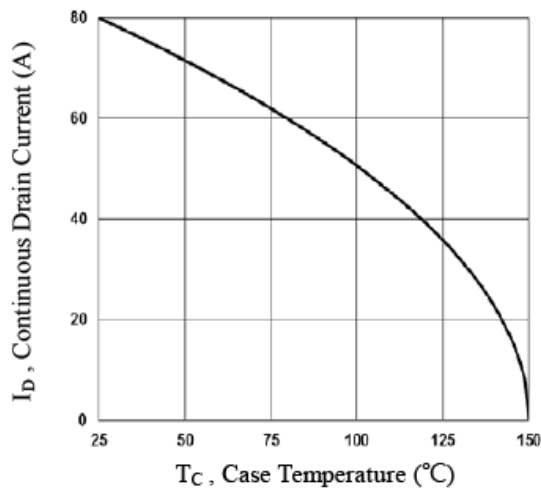
Symbol	Parameter	Typical	Unit
V <sub>DS</sub>	Drain-Source Voltage	30	V
V <sub>GS</sub>	Gate –Source Voltage	±20	V
I <sub>D</sub>	Continuous Drain Current	T <sub>A</sub> =25°C	80
		T <sub>A</sub> =100°C	51
I <sub>DM</sub>	Pulsed Drain Current	320	A
EAS	Single Pulse Avalanche Energy	125	mJ
IAS	Single Pulse Avalanche Current	50	A
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> =25°C)	66	W
	Power Dissipation (Derate above 25°C)	0.53	W/°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to +175	°C
T <sub>STG</sub>	Storage Temperature Range	-55 to +175	°C
R <sub>θJA</sub>	Thermal Resistance-Junction to Ambient	62	°C/W
R <sub>θJC</sub>	Thermal Resistance-Junction to Case	2	°C/W

## Electrical Characteristics

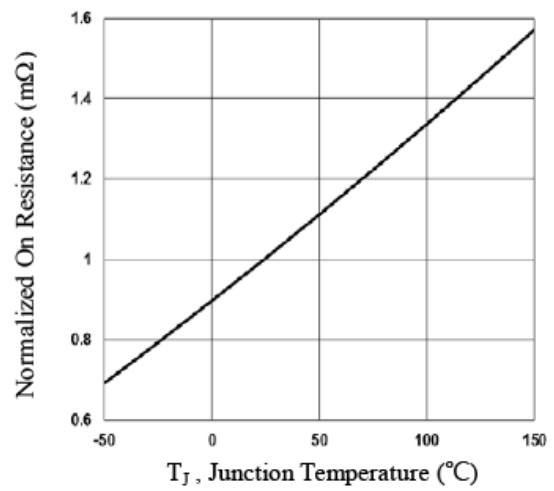
T<sub>A</sub>=25°C Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30			V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA		0.03		V/°C
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1.2	1.6	2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient			-5		mV/°C
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V			1	uA
		V <sub>DS</sub> =24V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C			10	
I <sub>S</sub>	Continuous Source Current	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current			80	A
I <sub>SM</sub>	Pulsed Source Current				320	
R <sub>DS(on)</sub>	Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =24A		2.9	3.8	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =12A		4.3	5.5	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =10A		28		S
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =1A			1	V
EAS	Single Pulse Avalanche Energy	V <sub>DD</sub> =25V, L=0.1mH, IAS=24A	31			mJ
<b>Dynamic</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =24A		24	34	nC
Q <sub>gs</sub>	Gate-Source Charge			4.2	6	
Q <sub>gd</sub>	Gate-Drain Charge			13	18	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		2200	3190	pF
C <sub>oss</sub>	Output Capacitance			280	405	
C <sub>rss</sub>	Reverse Transfer Capacitance			177	255	
t <sub>d(on)</sub>	Turn-On Time	V <sub>DD</sub> =15V, I <sub>D</sub> =15A, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω		12.6	24	ns
t <sub>r</sub>				19.5	37	
t <sub>d(off)</sub>	Turn-Off Time			42.8	81	
t <sub>f</sub>				13.2	25	
R <sub>g</sub>	Gate Resistance		V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		2	

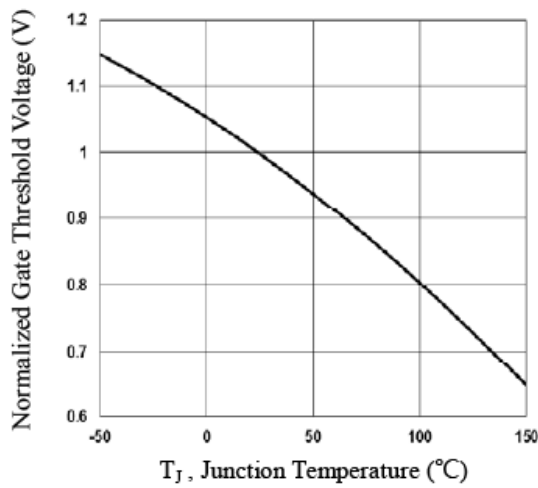
## Typical Performance Characteristics



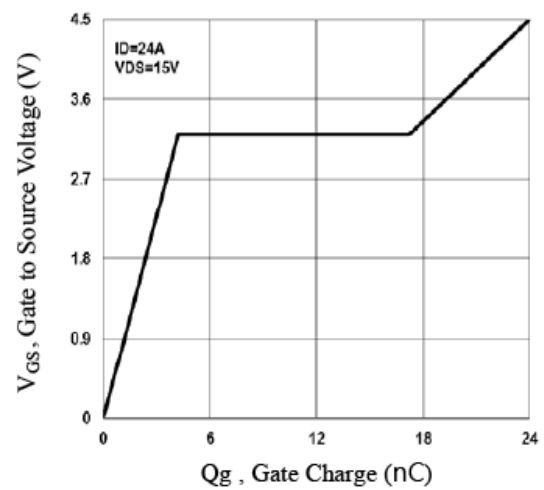
**Fig.1 Continuous Drain Current vs.  $T_C$**



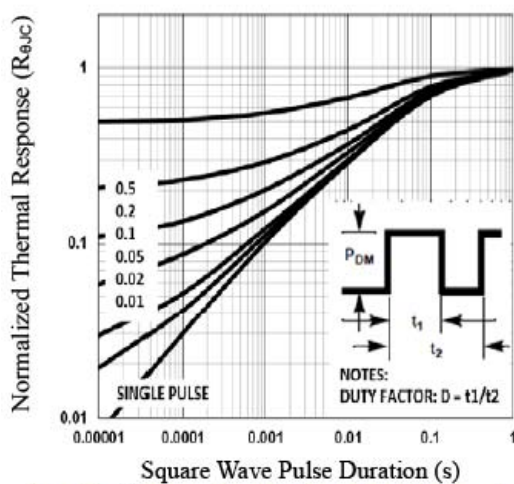
**Fig.2 Normalized RDSON vs.  $T_J$**



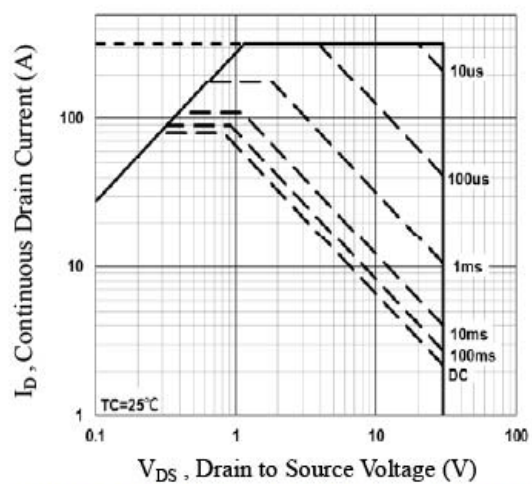
**Fig.3 Normalized  $V_{th}$  vs.  $T_J$**



**Fig.4 Gate Charge Waveform**



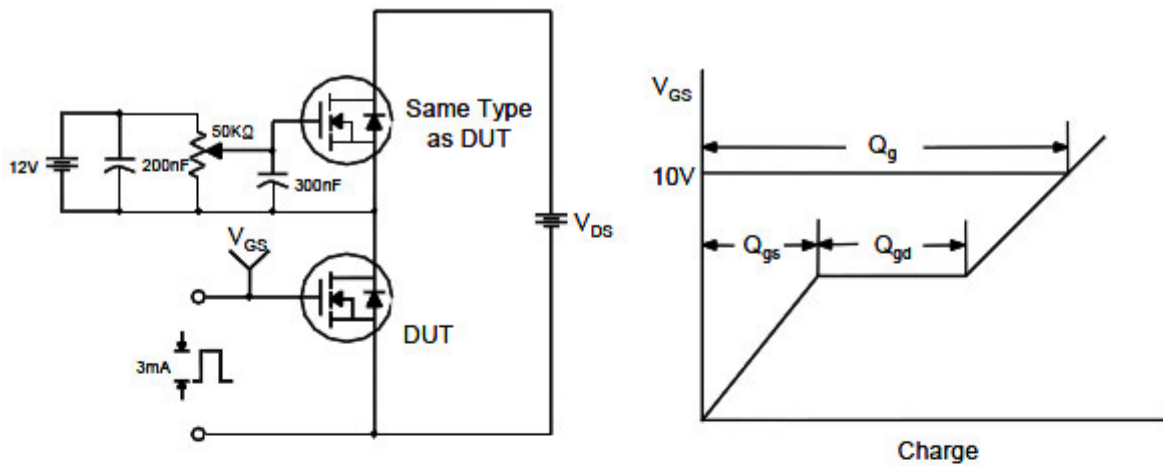
**Fig.5 Normalized Transient Impedance**



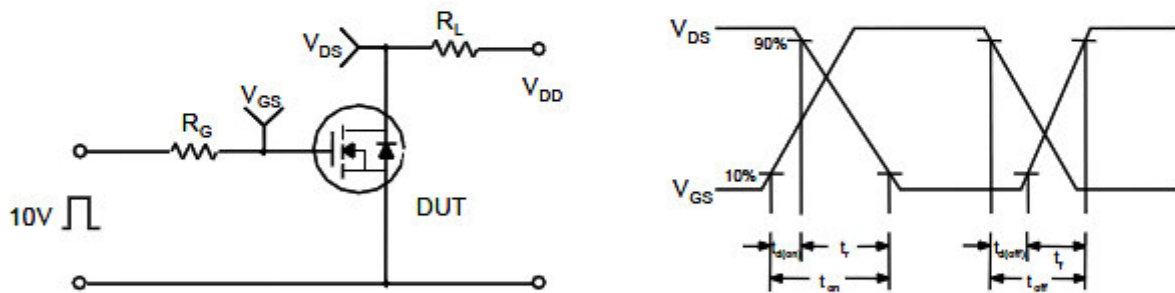
**Fig.6 Maximum Safe Operation Area**

## Typical Performance Characteristics (Continue)

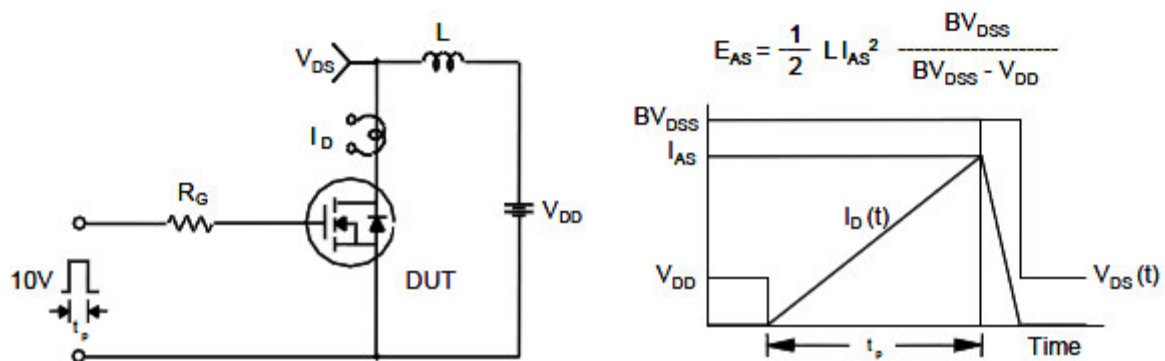
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

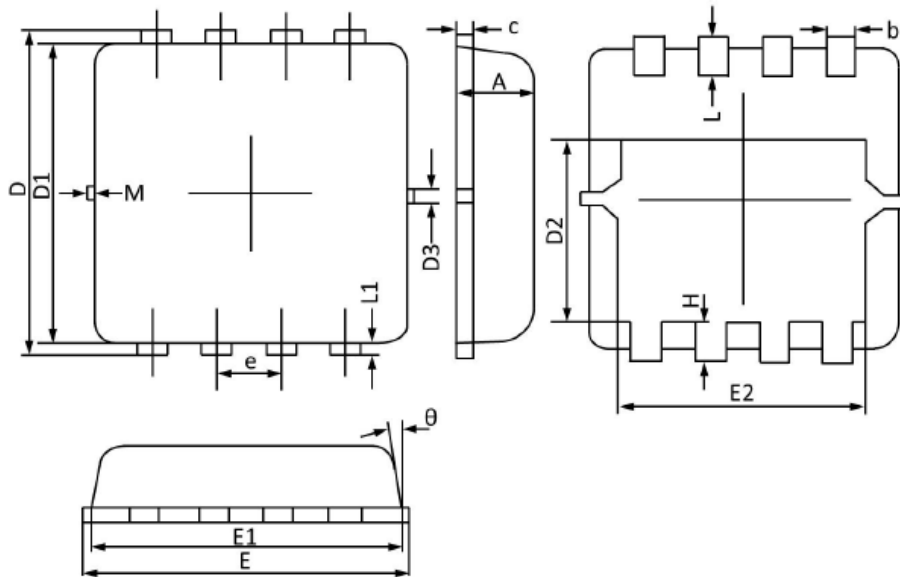


Unclamped Inductive Switching Test Circuit & Waveforms



## Package Dimension

### DFN3X3-8L







### Dimensions




Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
b	0.250	0.350	0.010	0.013
c	0.100	0.250	0.004	0.009
D	3.250	3.450	0.128	0.135
D1	3.000	3.200	0.119	0.125
D2	1.780	1.980	0.070	0.077
D3	0.130 (REF)		0.005 (REF)	
E	3.200	3.400	0.126	0.133
E1	3.000	3.200	0.119	0.125
E2	2.390	2.590	0.094	0.102
e	0.650 (BSC)		0.026 (BSC)	
H	0.300	0.500	0.011	0.019
L	0.300	0.500	0.011	0.019
L1	0.130 (REF)		0.005 (REF)	
θ	0°	12°	0°	12°
M	0.150 (REF)		0.006 (REF)	



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