

GSMDC3801R

30V N-Channel MOSFETs

Product Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

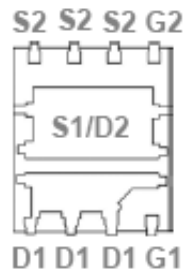
Features

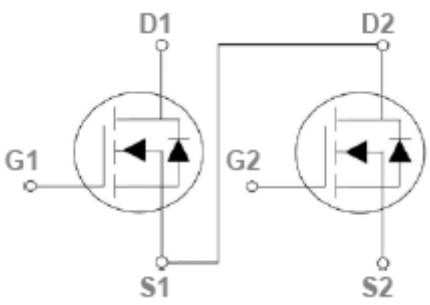
- 30V, 55A, $R_{DS(ON)}=9m\Omega@V_{GS}=10V$ (Q1)
- 30V, 80A, $R_{DS(ON)}=6m\Omega@V_{GS}=10V$ (Q2)
- Improved dv/dt capability
- Fast switching
- 100% EAS guaranteed
- Green Device Available
- DFN5X6-8L package design

Applications

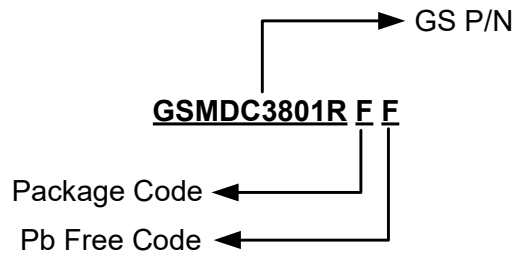
- MB / VGA / Vcore
- POL Buck Applications
- SMPS 2nd SR

Packages & Pin Assignments

GSMDC3801RFF (DFN5X6-8L)	
 <p style="text-align: center;">Bottom View</p>	
Pin	Description
1	Gate 1
2	Drain 1
3	Drain 1
4	Drain 1
5	Source 2
6	Source 2
7	Source 2
8	Gate 2

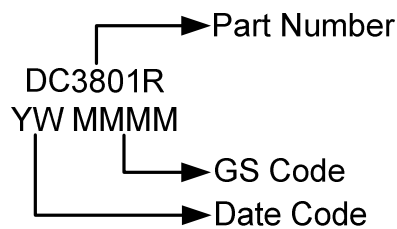


Ordering Information



Part Number	Package	Quantity
GSMDC3801RFF	DFN5x6-8L	3000pcs

Marking Information



Absolute Maximum Ratings

$T_C=25^{\circ}\text{C}$ Unless otherwise noted

Symbol	Parameter	Q1	Q2	Unit	
V_{DS}	Drain-Source Voltage	30	30	V	
V_{GS}	Gate-Source Voltage	± 20	± 20	V	
I_D	Continuous Drain Current, Chip/Package Limit	$T_C=25^{\circ}\text{C}$	55/10	80/15	A
		$T_C=100^{\circ}\text{C}$	35/6	51/9	
I_{DM}	Pulsed Drain Current, Chip/Package Limit ¹	220/40	320/60	A	
EAS	Single Pulse Avalanche Energy ²	45	88	mJ	
IAS	Single Pulse Avalanche Current ²	30	42	A	
P_D	Power Dissipation ($T_C=25^{\circ}\text{C}$)	40	54	W	
	Power Dissipation (Derate above 25°C)	0.32	0.43	W/ $^{\circ}\text{C}$	
T_J	Operating Junction Temperature Range	-55 to +150		$^{\circ}\text{C}$	
T_{STG}	Storage Temperature Range	-55 to +150		$^{\circ}\text{C}$	
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	62	62	$^{\circ}\text{C}/\text{W}$	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	3.1	2.3	$^{\circ}\text{C}/\text{W}$	

Electrical Characteristics (Q1)

T_J=25°C Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30			V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA		0.04		V/°C
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	1.6	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient			-4		mV/°C
I _{GSS}	Gate-Source Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Drain-Source Leakage Current	V _{DS} =30V, V _{GS} =0V			1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =125°C			10	
I _S	Continuous Source Current	V _G =V _D =0V, Force Current			55	A
I _{SM}	Pulsed Source Current				220	
R _{DS(on)}	Drain-Source On-Resistance	V _{GS} =10V, I _D =8A		7.5	9	mΩ
		V _{GS} =4.5V, I _D =5A		10	13	
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =8A		14		S
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =1A			1	V
EAS	Single Pulse Avalanche Energy	V _{DD} =25V, L=0.1mH, IAS=15A	12			mJ
Dynamic						
Q _g	Total Gate Charge ^{3,4}	V _{DS} =15V, V _{GS} =4.5V, I _D =20A		7.5		nC
Q _{gs}	Gate-Source Charge ^{3,4}			1.3		
Q _{gd}	Gate-Drain Charge ^{3,4}			4.5		
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		750		pF
C _{oss}	Output Capacitance			150		
C _{rss}	Reverse Transfer Capacitance			110		
t _{d(on)}	Turn-On Time ^{3,4}	V _{DD} =15V, I _D =15A, V _{GS} =10V, R _G =3.3Ω		4.8		ns
t _r				12.5		
t _{d(off)}	Turn-Off Time ^{3,4}			27.6		
t _f				8.2		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		2.7		Ω

Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V_{DD}=25V, V_{GS}=10V, L=0.1mH, Q1: I_{AS}=30A, Q2: I_{AS}=42A, R_G=25Ω, Starting T_J=25°C.
3. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
4. Essentially independent of operating temperature.

Electrical Characteristics (Q2)

T_J=25°C Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30			V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA		0.04		V/°C
V _{GS(th)}	Gate Threshold Voltage		1	1.6	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient	V _{DS} =V _{GS} , I _D =250uA		-4		mV/°C
I _{GSS}	Gate-Source Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Drain-Source Leakage Current	V _{DS} =30V, V _{GS} =0V			1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =125°C			10	
I _S	Continuous Source Current	V _G =V _D =0V, Force Current			80	A
I _{SM}	Pulsed Source Current				320	
R _{DS(on)}	Drain-Source On-Resistance	V _{GS} =10V, I _D =12A		4.8	6	mΩ
		V _{GS} =4.5V, I _D =8A		6.5	9	
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =10A		18		S
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =1A			1	V
EAS	Single Pulse Avalanche Energy	V _{DD} =25V, L=0.1mH, IAS=15A	20			mJ
Dynamic						
Q _g	Total Gate Charge ^{3,4}	V _{DS} =15V, V _{GS} =4.5V, I _D =20A		11.1		nC
Q _{gs}	Gate-Source Charge ^{3,4}			1.85		
Q _{gd}	Gate-Drain Charge ^{3,4}			6.8		
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		1160		pF
C _{oss}	Output Capacitance			200		
C _{rss}	Reverse Transfer Capacitance			180		
t _{d(on)}	Turn-On Time ^{3,4}	V _{DD} =15V, I _D =15A, V _{GS} =10V, R _G =3.3Ω		7.5		ns
t _r				14.5		
t _{d(off)}	Turn-Off Time ^{3,4}			35.2		
t _f				9.6		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		2.5		Ω

Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V_{DD}=25V, V_{GS}=10V, L=0.1mH, Q1: IAS=30A, Q2: IAS=42A, R_G=25Ω, Starting T_J=25°C.
3. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
4. Essentially independent of operating temperature.

Typical Performance Characteristics (Q1)

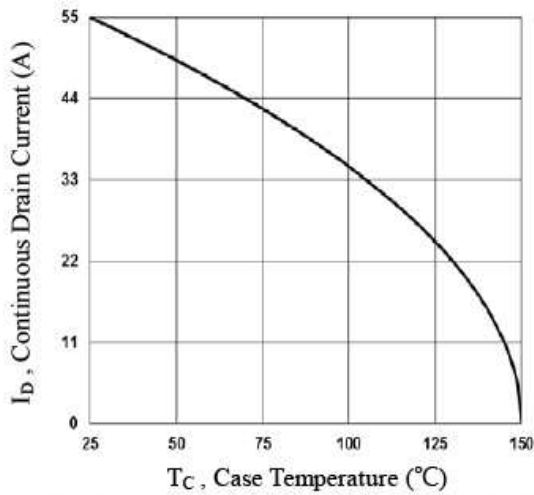


Fig.1 Q1 Continuous Drain Current vs. T_C

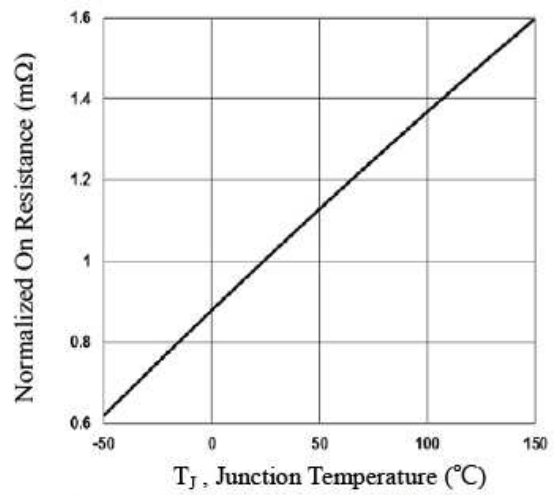


Fig.2 Q1 Normalized $R_{DS(on)}$ vs. T_J

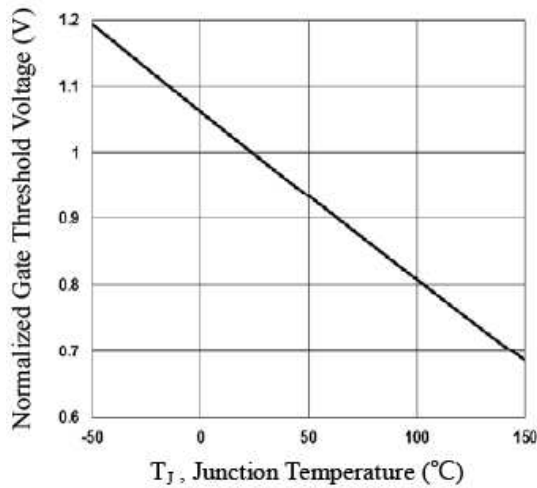


Fig.3 Q1 Normalized V_{th} vs. T_J

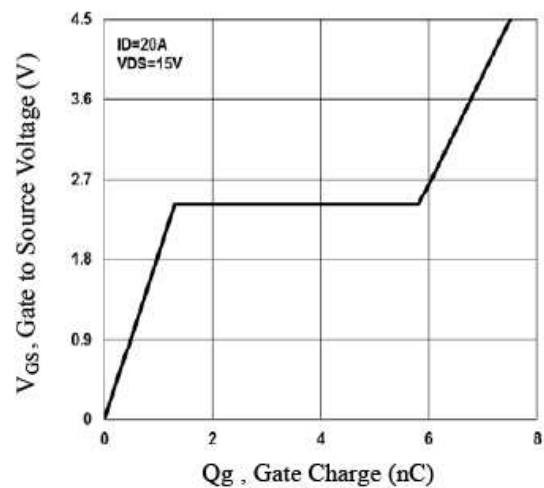


Fig.4 Q1 Gate Charge Waveform

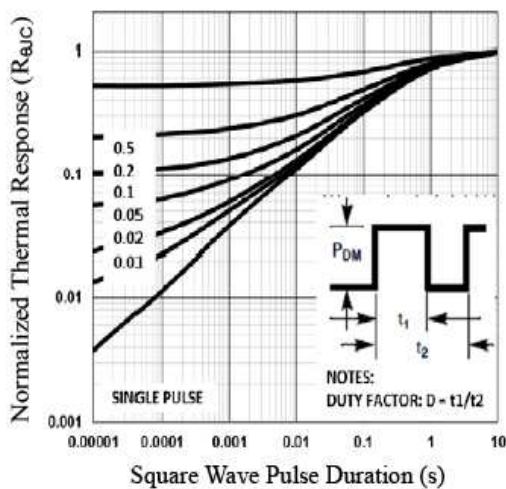


Fig.5 Q1 Normalized Transient Impedance

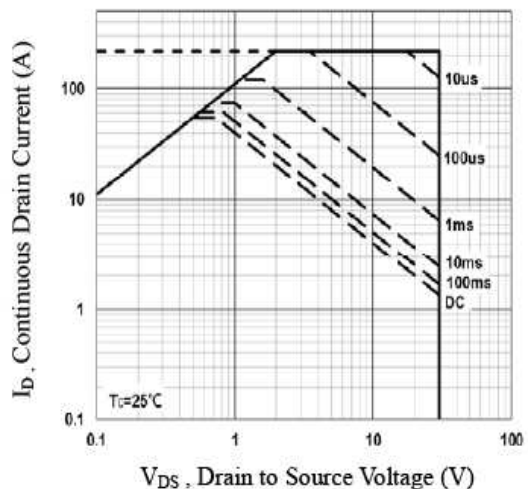


Fig.6 Q1 Maximum Safe Operation Area

Typical Performance Characteristics (Q2)

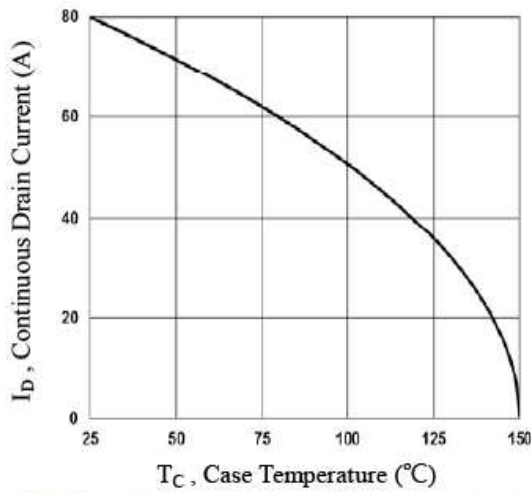


Fig.7 Q2 Continuous Drain Current vs. T_C

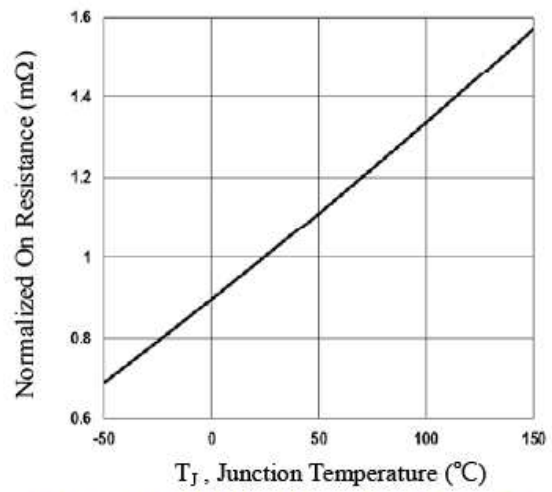


Fig.8 Q2 Normalized $R_{DS(on)}$ vs. T_J

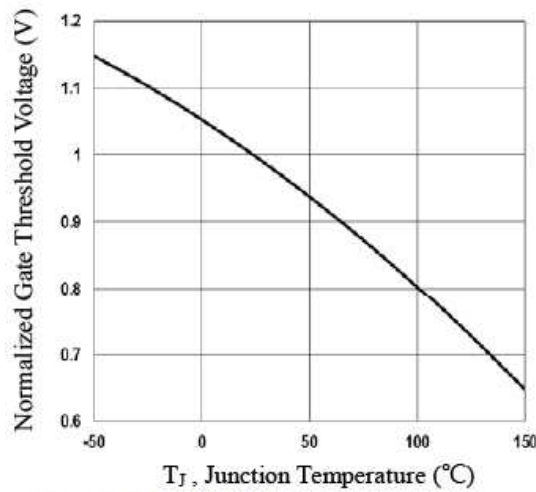


Fig.9 Q2 Normalized V_{th} vs. T_J

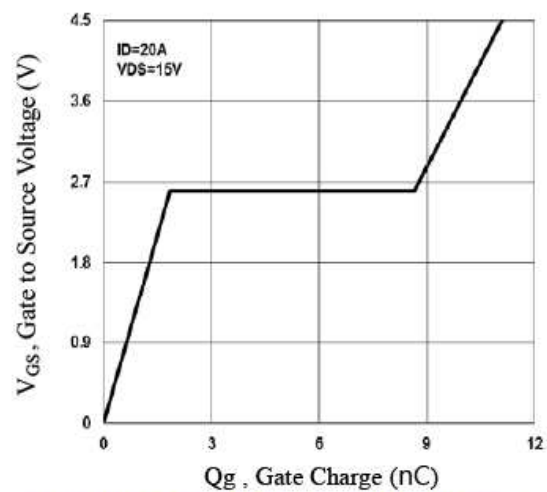


Fig.10 Q2 Gate Charge Waveform

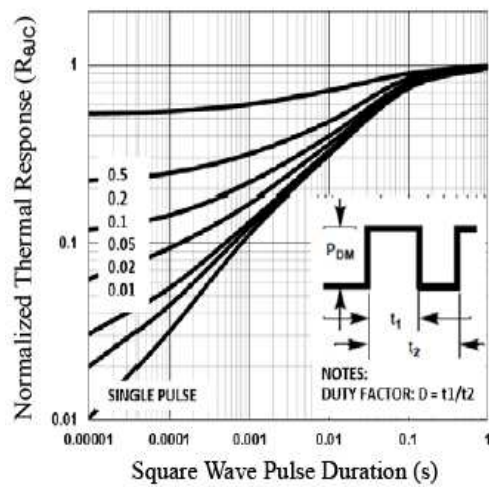


Fig.11 Q2 Normalized Transient Impedance

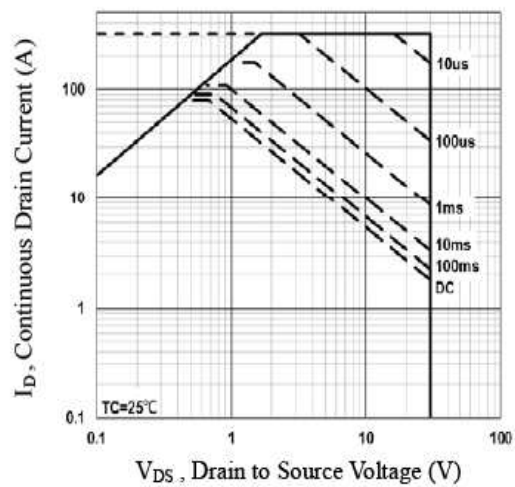
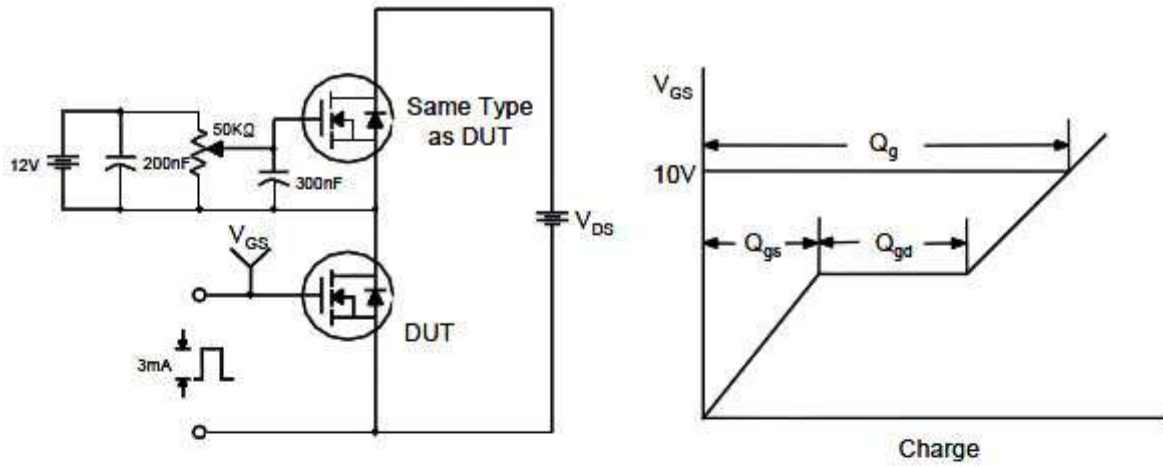


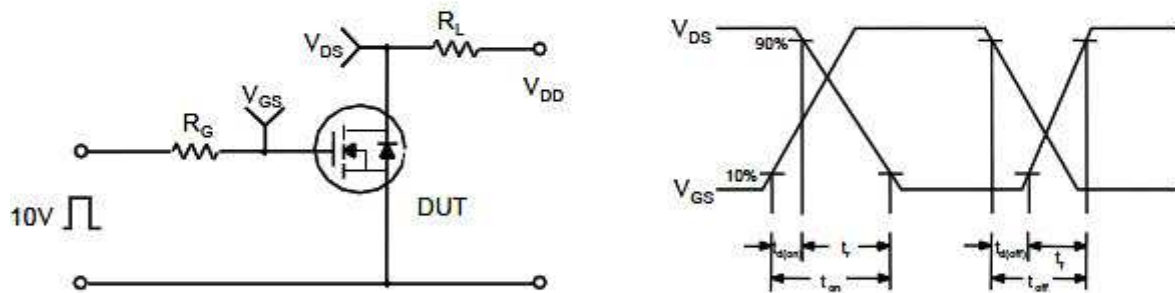
Fig.12 Q2 Maximum Safe Operation Area

Typical Performance Characteristics (Continue)

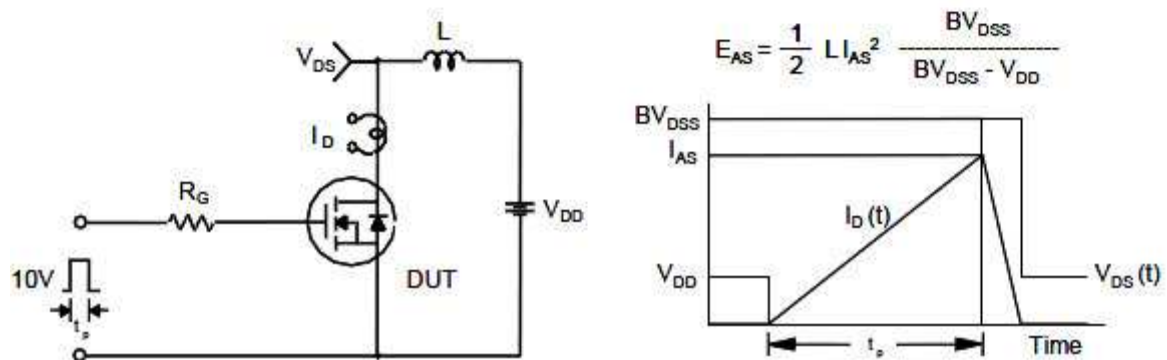
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

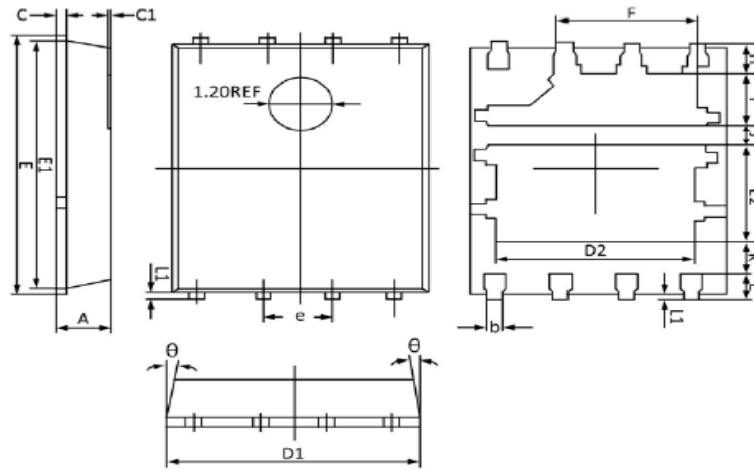


Unclamped Inductive Switching Test Circuit & Waveforms



Package Dimension

DFN5X6-8L









Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.036	0.043
b	0.330	0.510	0.013	0.020
C	0.200	0.300	0.008	0.011
C1	0.040 REF		0.002 REF	
D1	4.800	5.000	0.189	0.196
D2	3.610	3.960	0.143	0.155
E	5.900	6.100	0.233	0.240
E1	5.700	5.800	0.225	0.228
E2	2.020	2.420	0.080	0.095
e	1.270 BSC		0.050 BSC	
F	2.550	2.900	0.101	0.114
H	0.610	0.810	0.025	0.031
I	1.100	1.300	0.044	0.051
J	0.400	0.600	0.016	0.023
K	0.500	-	0.020	-
L	0.510	0.710	0.020	0.027
L1	0.060	0.200	0.003	0.007
θ	0°	12°	0°	12°

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CONTACT US

GS Headquarter	
	4F.,No.43-1,Lane11,Sec.6,Minquan E.Rd Neihu District Taipei City 114, Taiwan (R.O.C)
	886-2-2657-9980
	886-2-2657-3630
	sales_twn@gs-power.com

RD Division	
	824 Bolton Drive Milpitas. CA. 95035
	1-408-457-0587