

GSMDC0956Z

100V N-Channel MOSFETs

Product Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

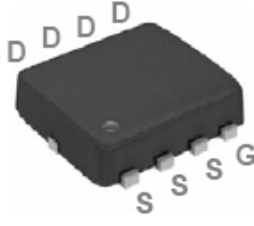
Features

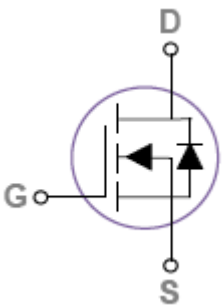
- 100V, 10A, $R_{DS(ON)}=115m\Omega@V_{GS}=10V$
- Improved dv/dt capability
- Fast switching
- 100% EAS guaranteed
- Green Device Available
- DFN3X3-8L package design

Applications

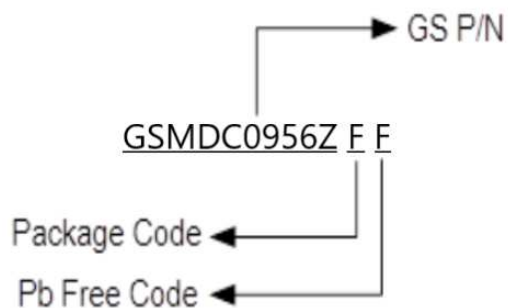
- Motor Drive
- Power Tools
- LED Lighting

Packages & Pin Assignments

GSMDC0956ZFF (DFN3X3-8L)	
 <p style="text-align: center;">Top View</p>	
Pin	Description
1	Source
2	Source
3	Source
4	Gate
5	Drain
6	Drain
7	Drain
8	Drain

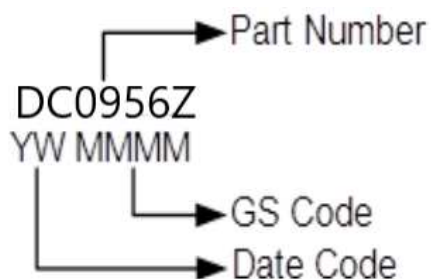


Ordering Information



Part Number	Package	Quantity
GSMDC0956ZFF	DFN3X3-8L	5000 PCS

Marking Information



Absolute Maximum Ratings

$T_C=25^\circ\text{C}$ Unless otherwise noted

Symbol	Parameter	Typical	Unit
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C=25^\circ\text{C}$	10
		$T_C=100^\circ\text{C}$	6.3
I_{DM}	Pulsed Drain Current (Note 1)	40	A
EAS	Single Pulse Avalanche Energy (Note 2)	6	mJ
IAS	Single Pulse Avalanche Current (Note 2)	11	A
P_D	Power Dissipation ($T_C=25^\circ\text{C}$)	29.8	W
	Power Dissipation (Derate above 25°C)	0.24	W/ $^\circ\text{C}$
T_J	Operating Junction Temperature Range	-50 to +150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-50 to +150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	62	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance-Junction to Case	4.2	$^\circ\text{C}/\text{W}$

Note 1: Repetitive Rating: Pulsed width limited by maximum junction temperature.

Note 2: $V_{DD}=25\text{V}$, $V_{GS}=10\text{V}$, $L=0.1\text{mH}$, $I_{AS}=11\text{A}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$.

Electrical Characteristics

T_J=25°C Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100			V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA		0.09		V/°C
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1.2	1.6	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient			-5		mV/°C
I _{GSS}	Gate-Source Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Drain-Source Leakage Current	V _{DS} =60V, V _{GS} =0V			1	uA
		V _{DS} =48V, V _{GS} =0V, T _J =125°C			10	
I _S	Continuous Source Current	V _G =V _D =0V, Force Current			10	A
I _{SM}	Pulsed Source Current				20	
R _{DS(on)}	Drain-Source On-Resistance	V _{GS} =10V, I _D =10A		90	115	mΩ
		V _{GS} =4.5V, I _D =8A		95	120	
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =10A		8.7		S
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =1A			1	V
t _{rr}	Reverse Recovery Time (Note 3,4)	V _{GS} =0V, I _S =1A, di/dt=100A/us		38		ns
Q _{rr}	Reverse Recovery Charge (Note 3,4)			27		nC
Dynamic						
Q _g	Total Gate Charge (Note 3,4)	V _{DS} =50V, V _{GS} =10V, I _D =2A		20	40	nC
Q _{gs}	Gate-Source Charge (Note 3,4)			3.2	6	
Q _{gd}	Gate-Drain Charge (Note 3,4)			3.6	7	
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		1400	2800	pF
C _{oss}	Output Capacitance			60	120	
C _{rss}	Reverse Transfer Capacitance			35	70	
t _{d(on)}	Turn-On Time (Note 3,4)	V _{DD} =50V, I _D =1A, V _{GS} =10V, R _G =3.3Ω		18	36	ns
t _r				4	8	
t _{d(off)}	Turn-Off Time (Note 3,4)			40	80	
t _f				3	6	
R _g	Gate Resistance		V _{DS} =0V, V _{GS} =0V, f=1MHz		2	

Note 3: The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.

Note 4: Essentially independent of operating temperature.

Typical Performance Characteristics

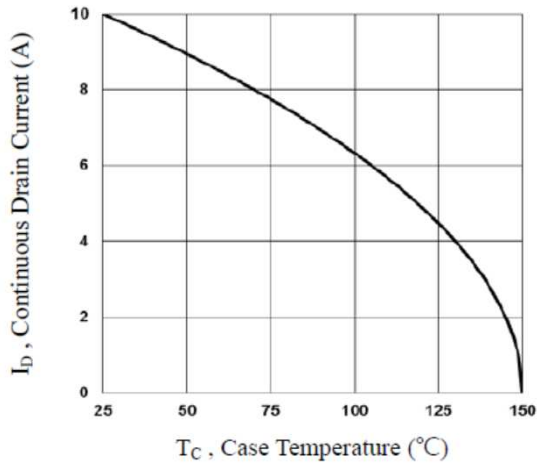


Fig.1 Continuous Drain Current vs. T_c

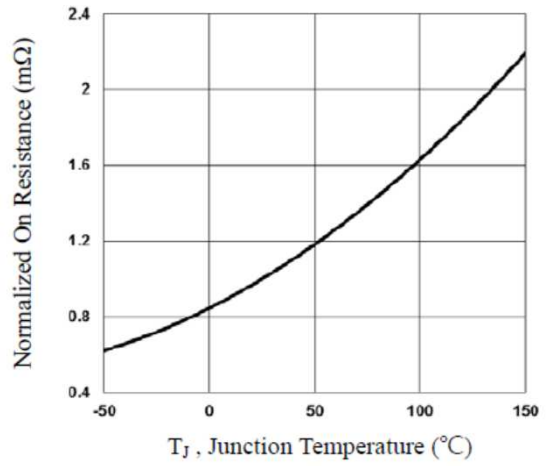


Fig.2 Normalized $R_{DS(on)}$ vs. T_j

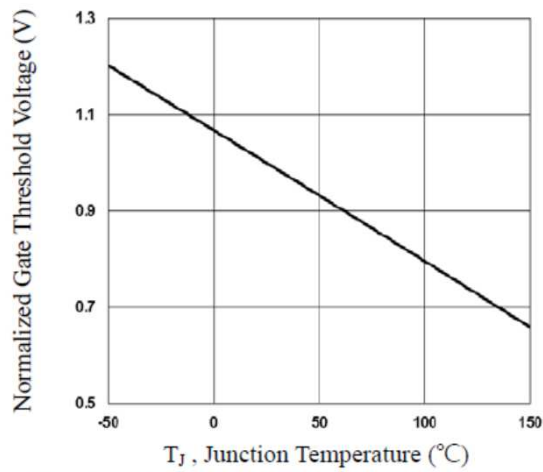


Fig.3 Normalized V_{th} vs. T_j

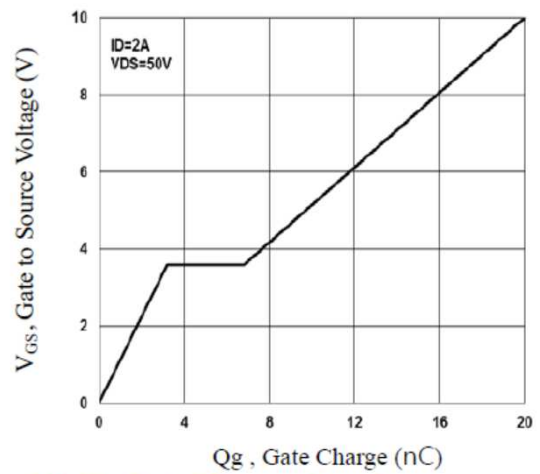


Fig.4 Gate Charge Waveform

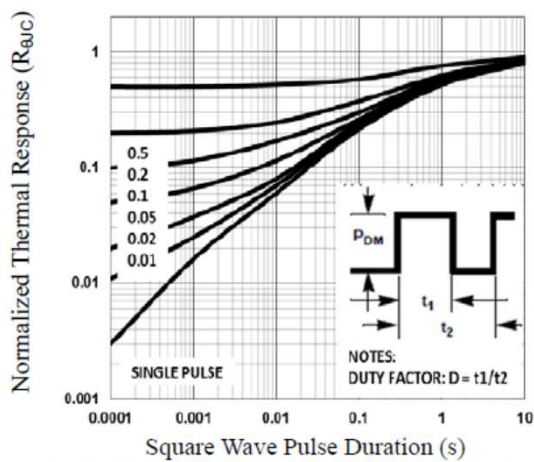


Fig.5 Normalized Transient Impedance

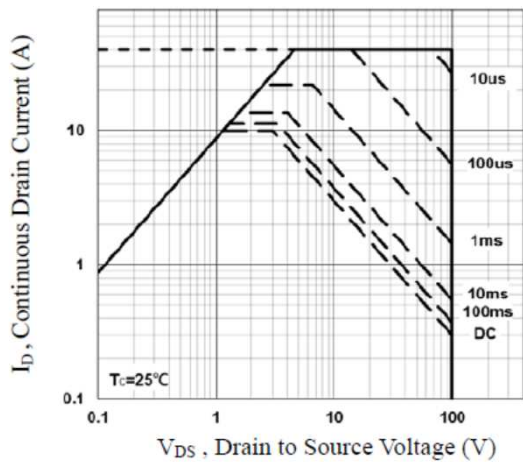
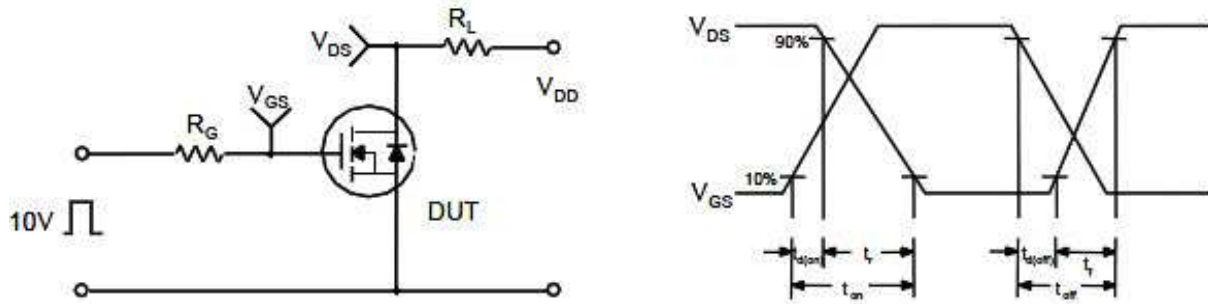


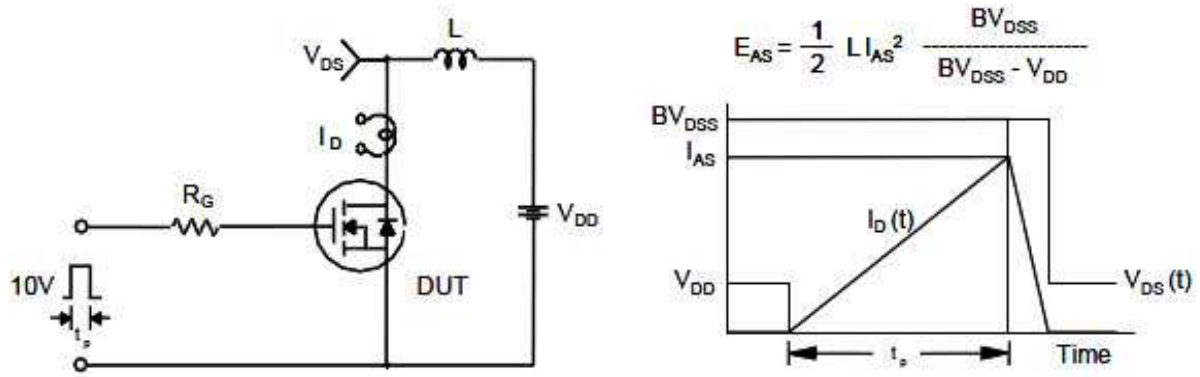
Fig.6 Maximum Safe Operation Area

Typical Performance Characteristics (Continue)

Resistive Switching Test Circuit & Waveforms

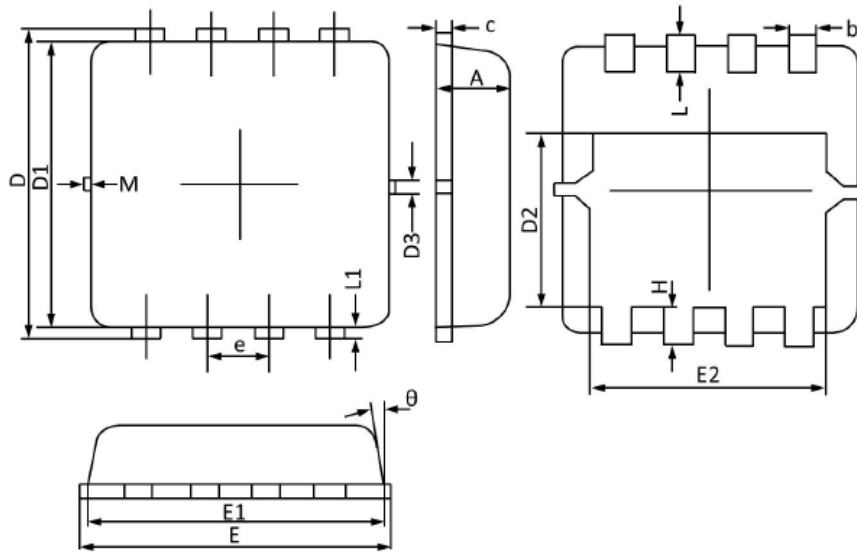


Unclamped Inductive Switching Test Circuit & Waveforms



Package Dimension

DFN3X3-8L









Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
b	0.250	0.350	0.010	0.013
c	0.100	0.250	0.004	0.009
D	3.250	3.450	0.128	0.135
D1	3.000	3.200	0.119	0.125
D2	1.780	1.980	0.070	0.077
D3	0.130 (REF)		0.005 (REF)	
E	3.200	3.400	0.126	0.133
E1	3.000	3.200	0.119	0.125
E2	2.390	2.590	0.094	0.102
e	0.650 (BSC)		0.026 (BSC)	
H	0.300	0.500	0.011	0.019
L	0.300	0.500	0.011	0.019
L1	0.130 (REF)		0.005 (REF)	
θ	0°	12°	0°	12°
M	0.150 (REF)		0.006 (REF)	

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CONTACT US

GS Headquarter	
	4F.,No.43-1,Lane11,Sec.6,Minquan E.Rd Neihu District Taipei City 114, Taiwan (R.O.C)
	886-2-2657-9980
	886-2-2657-3630
	sales_twn@gs-power.com

RD Division	
	824 Bolton Drive Milpitas. CA. 95035
	1-408-457-0587