GSMDB2116SFF

20V N+P Dual Channel MOSFETs

Product Description

These N+P dual Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

Features

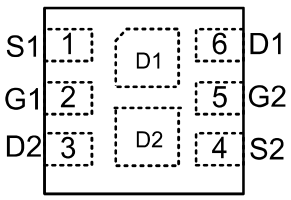
- N-Channel
  20V, 5A, $R_{DS(ON)}$=40mΩ@V_{GS}=4.5V
- P-Channel
  -20V, -4.7A, $R_{DS(ON)}$=95mΩ@V_{GS}=-4.5V
- Fast switching
- Suit for -1.8V/1.8V Gate Drive Applications
- Green Device Available
- DFN2X2-6L(B) package design

Applications

- Notebook
- Load Switch
- Networking
- Hand-held Instruments

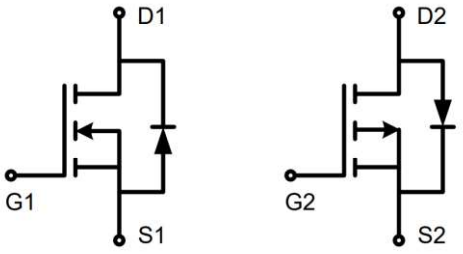
Packages & Pin Assignments

GSMDB2116SFF (DFN2X2-6L(B))



Top Views

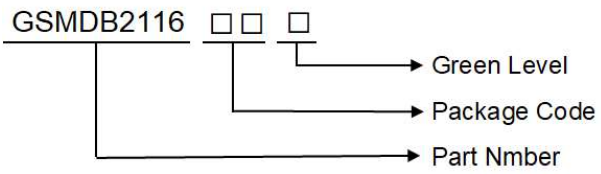
Pin	Description
1	Source 1
2	Gate 1
3	Drain 2
4	Source 2
5	Gate 2
6	Drain 1

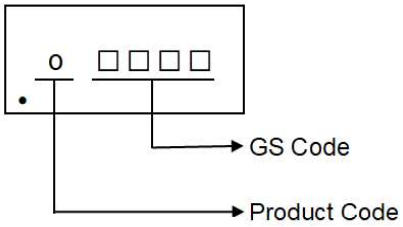


n-channel **p-channel**

Ordering and Marking Information

Part Number	Package	Marking	Quantity
GSMDB2116SFF	DFN2X2-6L(B)	o□□□□	4000pcs





- Package Code
  SF: DFN2x2-6L(B)
- Green Level
  F: RoHS and Halogen Free

Absolute Maximum Ratings

T_C=25ºC Unless otherwise noted

Symbol	Parameter		Typical N-Channel	Typical P-Channel	Unit
V_{DS}	Drain-Source Voltage		20	-20	V
V_{GS}	Gate-Source Voltage		±10	±10	V
I_D	Continuous Drain Current(T_J=150℃)	T_C=25℃	5	-4.7	A
		T_C=100℃	4.1	-3.9	
I_{DM}	Pulsed Drain Current (Note 1)		15.2	-10	A
P_D	Power Dissipation	T_C=25℃	1.56		W
		Derate above 25℃	0.01		W/℃
T_J	Operating Junction Temperature Range		-55 to +150		℃
T_{STG}	Storage Temperature Range		-55 to +150		℃
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		80		℃/W
$R_{\theta JC}$	Thermal Resistance-Junction to Case		15		℃/W

Note 1: Repetitive Rating: Pulsed width limited by maximum junction temperature.

Electrical Characteristics (N-Channel)

T_J=25℃ Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=250uA	20			V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃, I_D=1mA		0.02		V/℃
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250uA	0.3	0.6	1.0	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient			-2		mV/℃
I_{GSS}	Gate Leakage Current	V_{DS}=0V,V_{GS}=±10V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V,V_{GS}=0V			1	uA
		V_{DS}=16V,V_{GS}=0V, T_J=125℃			10	
I_S	Continuous Source Current	V_G=V_D=0V, Force Current			5	A
I_{SM}	Pulsed Source Current				10	
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=4.5V,I_D=3A		30	40	mΩ
		V_{GS}=2.5V,I_D=2A		42	55	
		V_{GS}=1.8V,I_D=1.5A		55	70	
g_{FS}	Forward Transconductance	V_{DS}=10V,I_D=2A		4.4		S
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_S=1A			1	V
Dynamic						
Q_g	Total Gate Charge	V_{DS}=10V,V_{GS}=4.5V, I_D=3A		5.8	10	nC
Q_{gs}	Gate-Source Charge			0.6	1.5	
Q_{gd}	Gate-Drain Charge			1.5	3	
C_{iss}	Input Capacitance	V_{DS}=15V,V_{GS}=0V, f=1MHz		315	600	pF
C_{oss}	Output Capacitance			50	80	
C_{rss}	Reverse Transfer Capacitance			40	60	
$t_{d(on)}$	Turn-On Time (Note 2,3)	V_{DD}=10V,I_D=1A, V_{GS}=4.5V,R_G=25Ω		2.9	6	ns
t_r				8.4	16	
$t_{d(off)}$	Turn-Off Time (Note 2,3)			19.2	38	
t_f				5.6	12	

Note 2: The data tested by pulsed, pulse width≦300us, duty cycle≦2%.

Note 3: Essentially independent of operating temperature.

Electrical Characteristics (P-Channel)

T_J=25℃ Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=-250uA	-20			V
△BV_{DSS}/△T_J	BV_{DSS} Temperature Coefficient	Reference to 25℃, I_D=-1mA		-0.01		V/℃
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250uA	-0.3	-0.6	-1.0	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient			3		mV/℃
I_{GSS}	Gate Leakage Current	V_{DS}=0V,V_{GS}=±10V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-20V,V_{GS}=0V			-1	uA
		V_{DS}=-16V,V_{GS}=0V, T_J=125℃			-10	
I_S	Continuous Source Current	V_G=V_D=0V, Force Current			-4.7	A
I_{SM}	Pulsed Source Current				-9.4	
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS} =-4.5V,I_D=-3A		80	95	mΩ
		V_{GS} =-2.5V,I_D=-2A		109	125	
		V_{GS} =-1.8V,I_D=-1A		148	161	
g_{FS}	Forward Transconductance	V_{DS}=-10V,I_D=-1A		2.2		S
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_S=-1A			-1	V
Dynamic						
Q_g	Total Gate Charge	V_{DS}=-10V,V_{GS}=-4.5V, I_D=-2A		4.8	10	nC
Q_{gs}	Gate-Source Charge			0.5	1	
Q_{gd}	Gate-Drain Charge			1.9	4	
C_{iss}	Input Capacitance	V_{DS}=-15V,V_{GS}=0V, f=1MHz		350	510	pF
C_{oss}	Output Capacitance			65	95	
C_{rss}	Reverse Transfer Capacitance			50	75	
$t_{d(on)}$	Turn-On Time (Note 2,3)	V_{DD}=-10V,I_D=-1A, V_{GS}=-4.5V,R_G=25Ω		3.5	7	ns
t_r				12.6	24	
$t_{d(off)}$	Turn-Off Time (Note 2,3)			32.6	62	
t_f				8.4	16	

Note 2: The data tested by pulsed, pulse width ≦300us, duty cycle ≦2%.

Note 3: Essentially independent of operating temperature.

Typical Performance Characteristics (N-Channel)

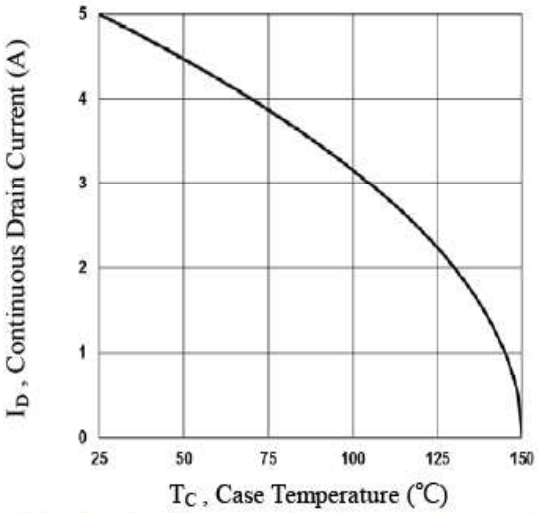


Fig.1 Continuous Drain Current vs. T_c

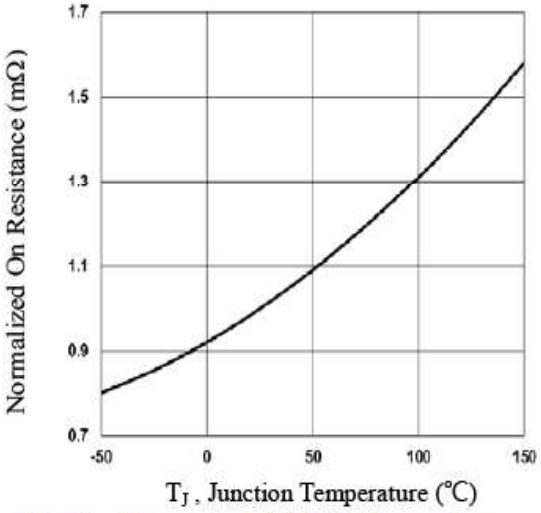


Fig.2 Normalized RDSON vs. T_J

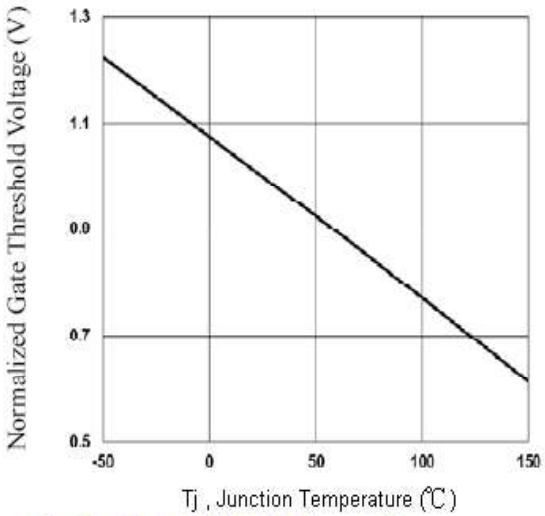


Fig.3 Normalized V_{th} vs. T_J

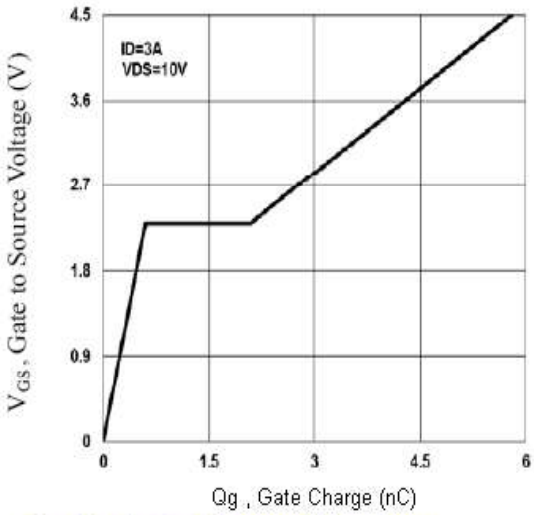


Fig.4 Gate Charge Waveform

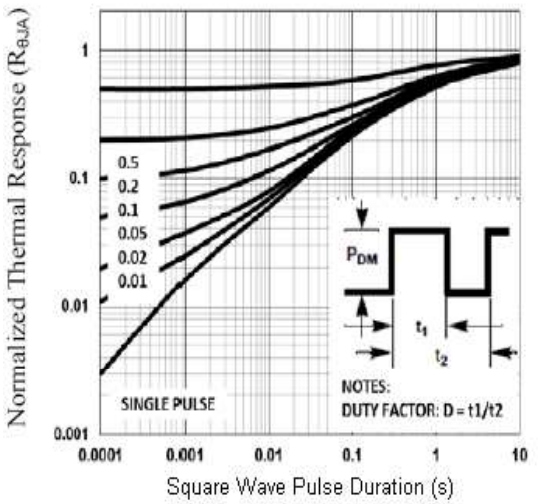


Fig.5 Normalized Transient Impedance

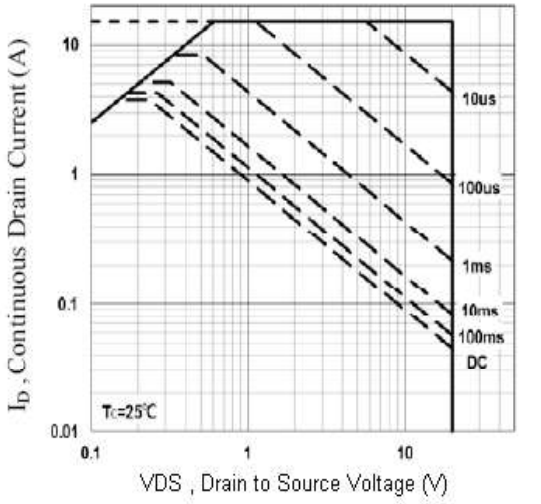
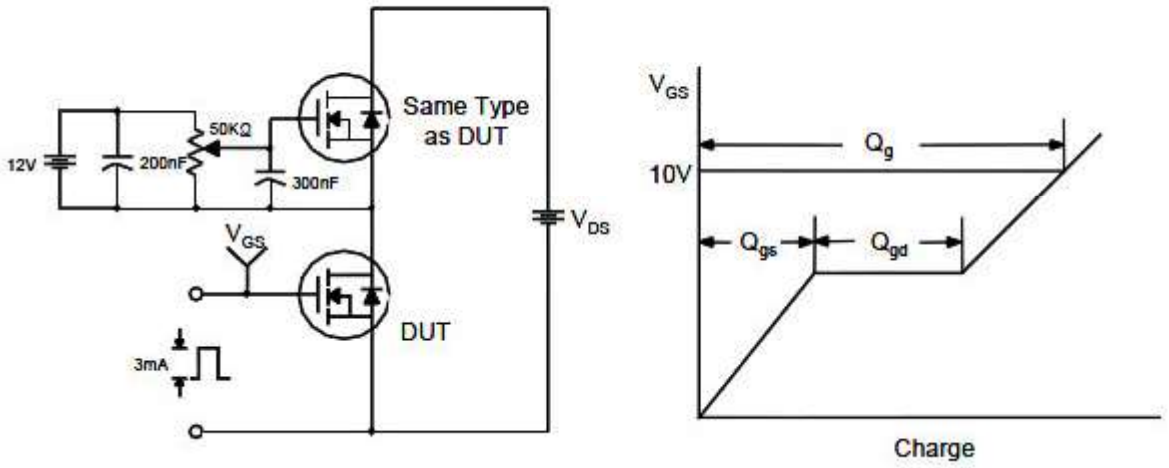


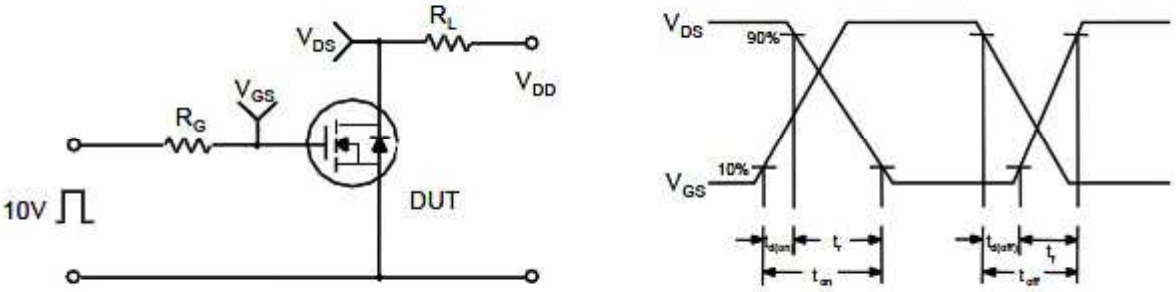
Fig.6 Maximum Safe Operation Area

Typical Performance Characteristics (N-Channel)

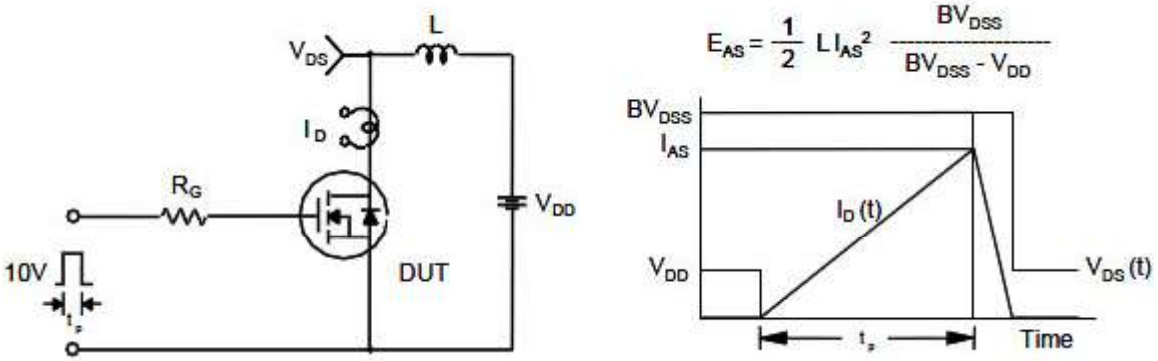
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Typical Performance Characteristics (P-Channel)

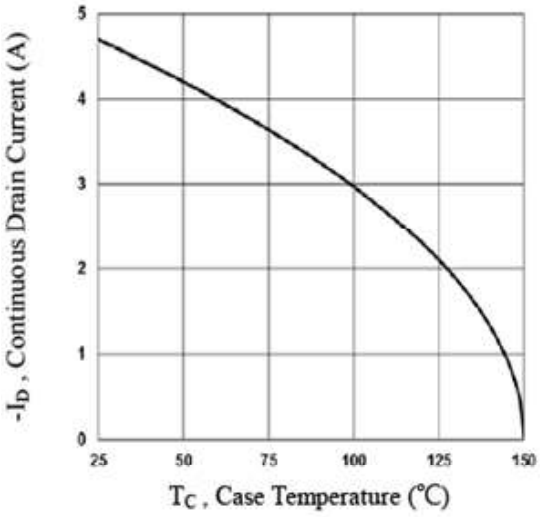


Fig.7 Continuous Drain Current vs. T_c

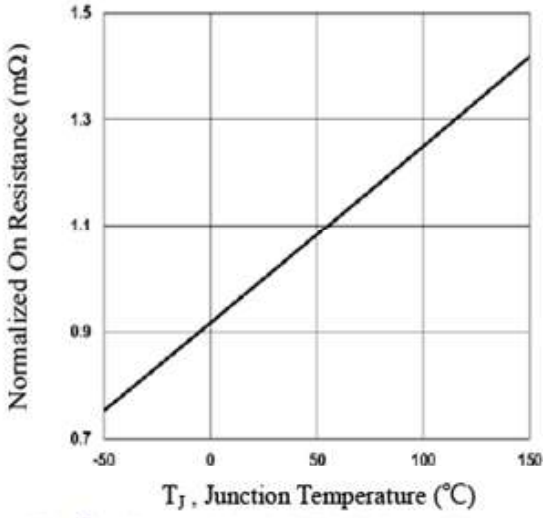


Fig.8 Normalized RDSON vs. T_J

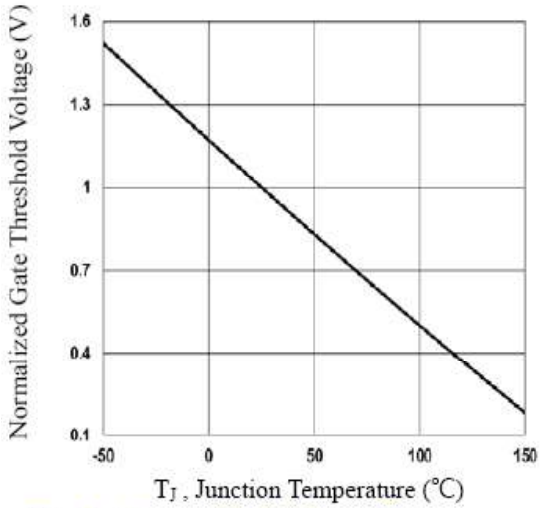


Fig.9 Normalized V_{th} vs. T_J

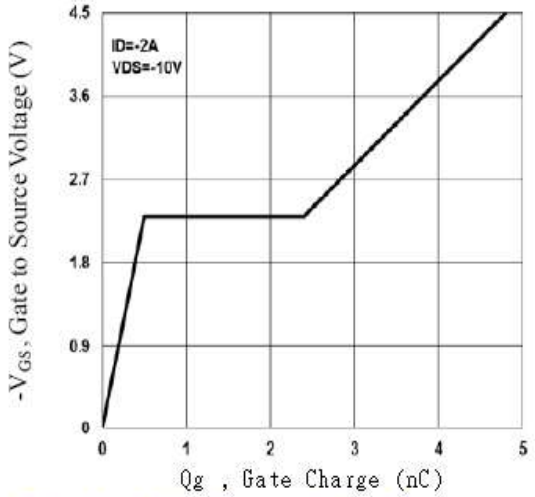


Fig.10 Gate Charge Waveform

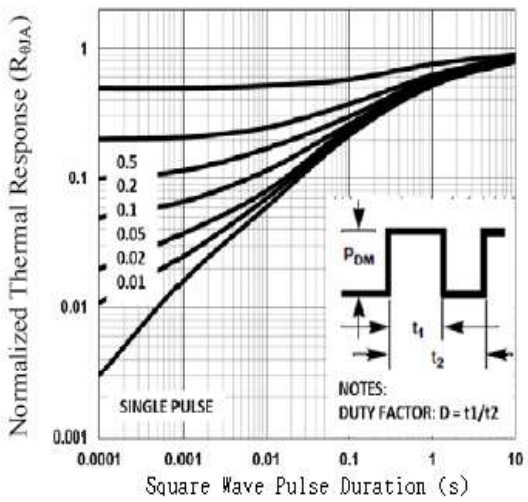


Fig.11 Normalized Transient Impedance

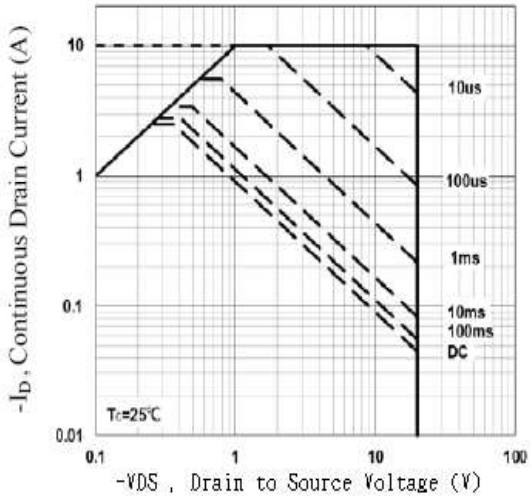
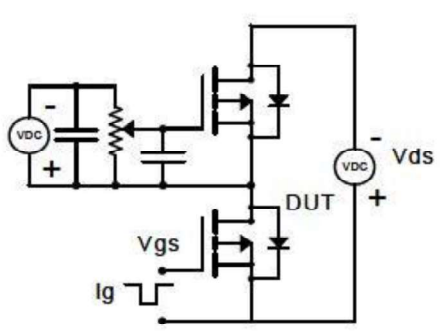
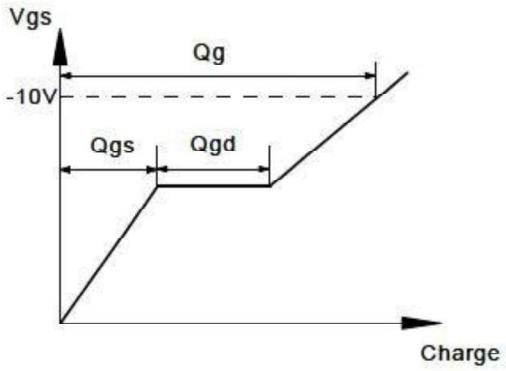


Fig.12 Maximum Safe Operation Area

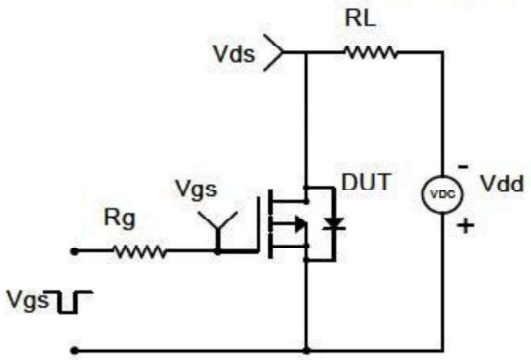
Typical Performance Characteristics (P-Channel)

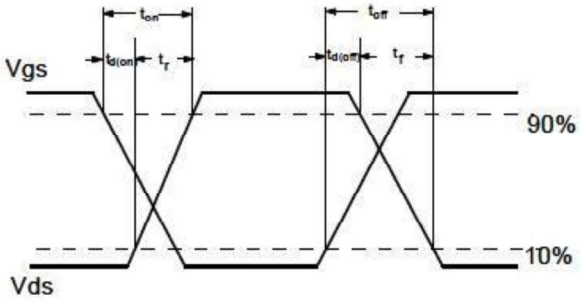
Gate Charge Test Circuit & Waveform



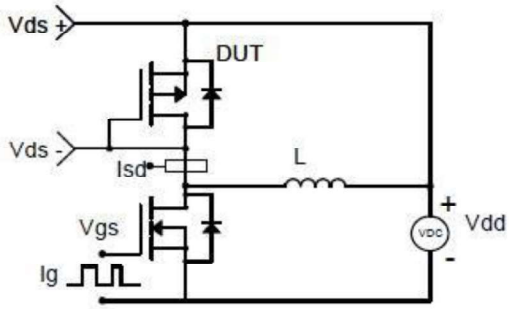


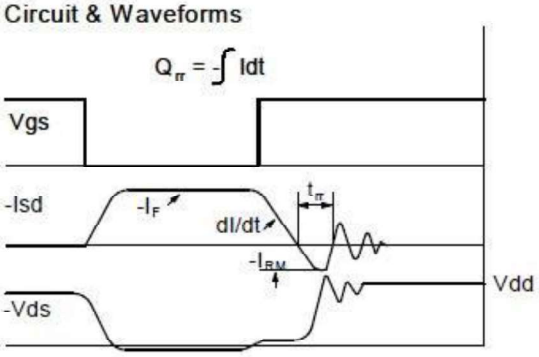
Resistive Switching Test Circuit & Waveforms





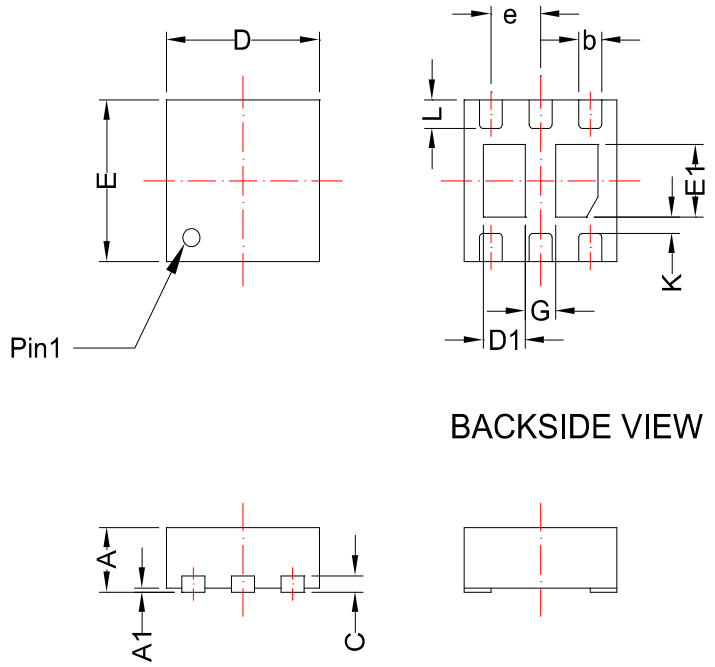
Diode Recovery Test Circuit & Waveforms



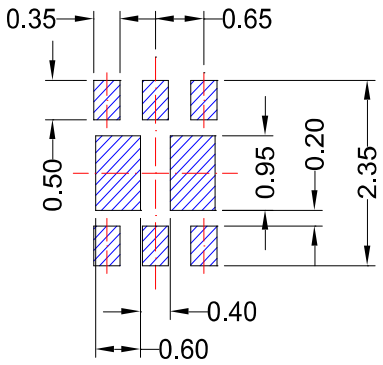


DFN2X2-6L(B)

Package Dimension



Recommended Land Pattern



Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.23	0.33	0.009	0.013
c	0.203 REF		0.008 REF	
D	1.95	2.05	0.077	0.081
D1	0.50	0.60	0.020	0.024
E	1.95	2.05	0.077	0.081
E1	0.85	0.95	0.033	0.037
e	0.65 BSC		0.026 BSC	
L	0.27	0.37	0.011	0.015
G	0.40 BSC		0.016 BSC	
K	0.20 Min.		0.008 Min.	

NOTE:

DIMENSION D AND E DO NOT INCLUDE MOLD FLASH,TIE BAR BURRS, GATE BURRS, AND INTERLEAD FLASH,NOT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

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