

GSMD35N15

150V N-Channel MOSFETs

Product Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

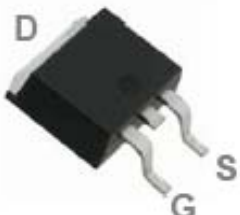
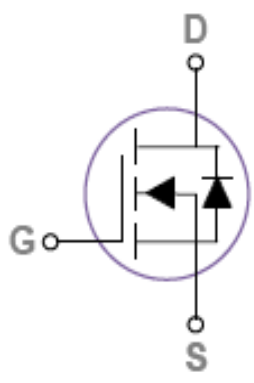
Features

- 150V, 35A, $R_{DS(ON)}=46m\Omega@V_{GS}=10V$
- Improved dv/dt capability
- Fast switching
- V_{GS} Guaranteed $\pm 25V$
- Green Device Available
- TO-252-2L package design

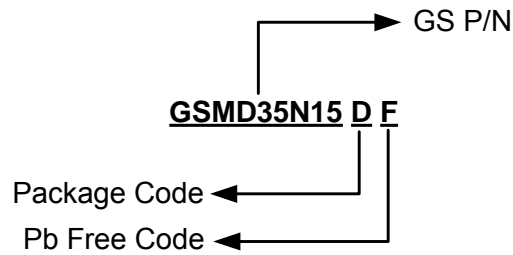
Applications

- Motor Drive
- DC-DC Switching
- LED Applications
- Power Tools

Packages & Pin Assignments

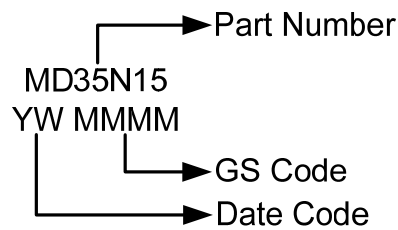
GSMD35N15DF (TO-252-2L)	
 <p>Top View</p>	
Description	
Gate	
Source	
Drain	

Ordering Information



Part Number	Package	Quantity Reel
GSMD35N15DF	TO-252-2L	2500 PCS

Marking Information



Absolute Maximum Ratings

$T_A=25^{\circ}\text{C}$ Unless otherwise noted

Symbol	Parameter	Typical	Unit
V_{DS}	Drain-Source Voltage	150	V
V_{GS}	Gate-Source Voltage	± 25	V
I_D	Continuous Drain Current	$T_A=25^{\circ}\text{C}$	35
		$T_A=100^{\circ}\text{C}$	22
I_{DM}	Pulsed Drain Current	140	A
EAS	Single Pulse Avalanche Energy	100	mJ
IAS	Single Pulse Avalanche Current	14.2	A
P_D	Power Dissipation ($T_A=25^{\circ}\text{C}$)	114	W
	Power Dissipation (Derate above 25°C)	0.91	W/ $^{\circ}\text{C}$
T_J	Operating Junction Temperature Range	-55 to +150	$^{\circ}\text{C}$
T_{STG}	Storage Temperature Range	-55 to +150	$^{\circ}\text{C}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	50	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance-Junction to Case	1.1	$^{\circ}\text{C}/\text{W}$

Note 1: Repetitive Rating : Pulsed width limited by maximum junction temperature.

Note 2: $V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$, $L=1\text{mH}$, $I_{AS}=10\text{A}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$.

Electrical Characteristics

T_A=25°C Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	150			V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA		0.09		V/°C
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient			-11		mV/°C
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±25V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =120V, V _{GS} =0V			1	μA
		V _{DS} =120V, V _{GS} =0V, T _J =85°C			30	
I _S	Continuous Source Current	V _G =V _D =0V, Force Current			35	A
I _{SM}	Pulsed Source Current				140	
R _{DS(on)}	Drain-Source On-Resistance	V _{GS} =10V, I _D =10A		35	46	mΩ
		V _{GS} =6V, I _D =8A		40	52	
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =1A			1	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =17A		53		S
t _{rr}	Reverse Recovery Time	V _{GS} =0V, I _S =1A, di/dt=100A/us		60		ns
Q _{rr}	Reverse Recovery Charge			165		nC
Dynamic						
Q _g	Total Gate Charge	V _{DS} =75V, V _{GS} =10V, I _D =10A		40	56	nC
Q _{gs}	Gate-Source Charge			9	14	
Q _{gd}	Gate-Drain Charge			12	18	
C _{iss}	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f=1MHz		1900	2760	pF
C _{oss}	Output Capacitance			200	290	
C _{rss}	Reverse Transfer Capacitance			87	130	
t _{d(on)}	Turn-On Time	V _{DD} =30V, I _D =1A, V _{GS} =10V, R _G =6Ω		16	29	ns
t _r				12	22	
t _{d(off)}	Turn-Off Time			48	87	
t _f				16	29	

Note 3: The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%.

Note 4: Essentially independent of operating temperature.

Typical Performance Characteristics

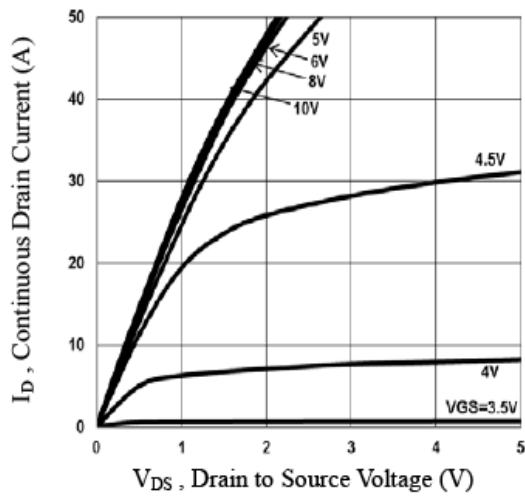


Fig.1 Output Characteristics

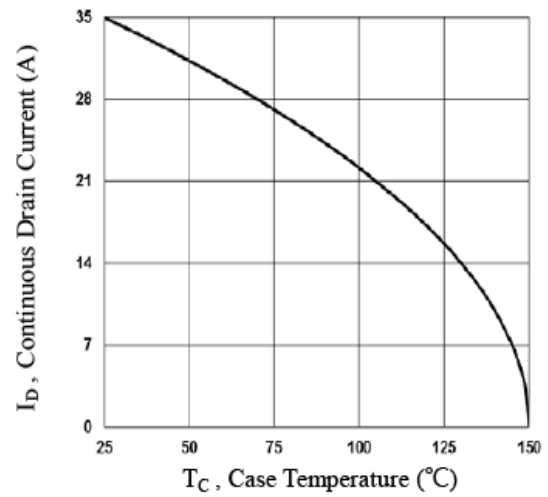


Fig.2 Continuous Drain Current vs. T_c

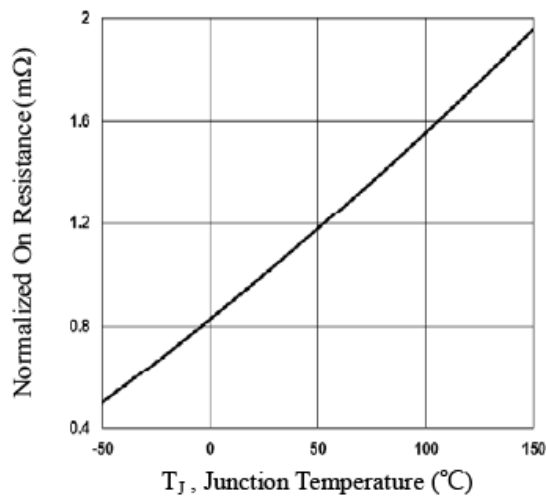


Fig.3 Normalized $R_{DS(on)}$ vs. T_j

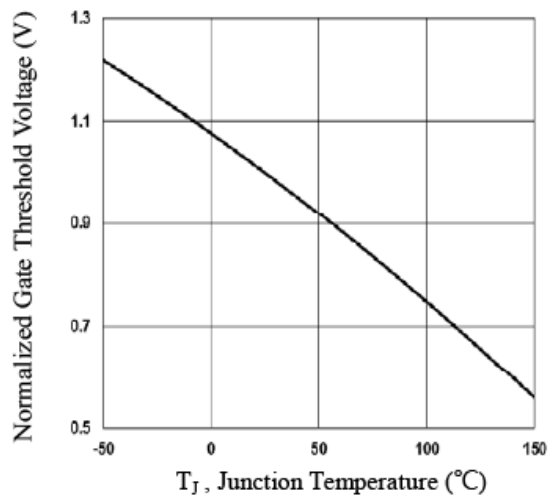


Fig.4 Normalized V_{th} vs. T_j

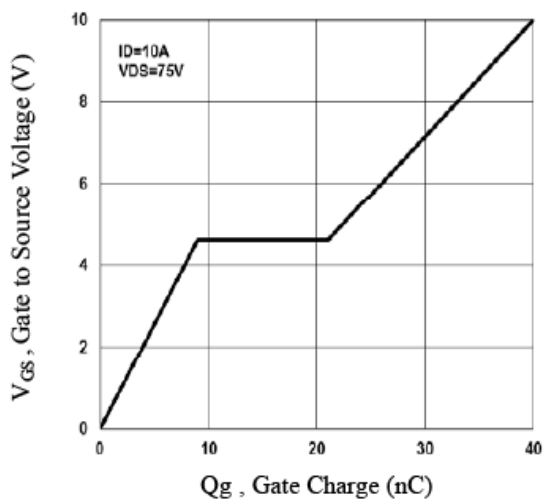


Fig.5 Gate Charge Waveform

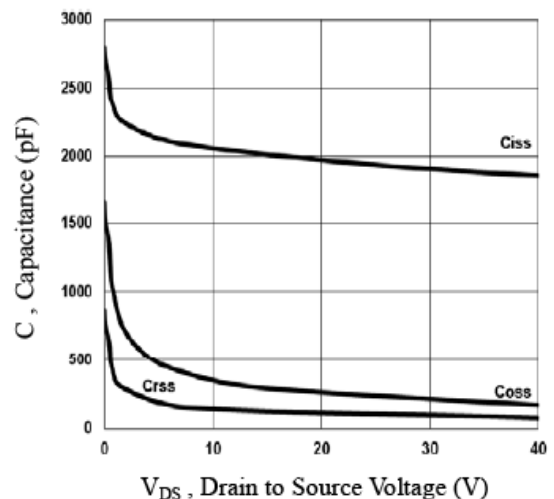


Fig.6 Capacitance Characteristics

Typical Performance Characteristics (Continue)

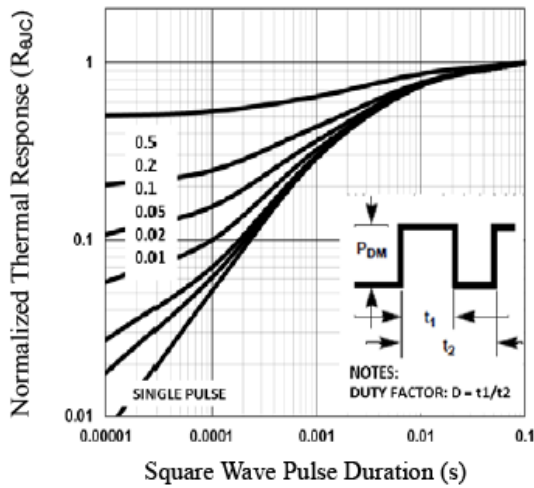


Fig.7 Normalized Transient Impedance

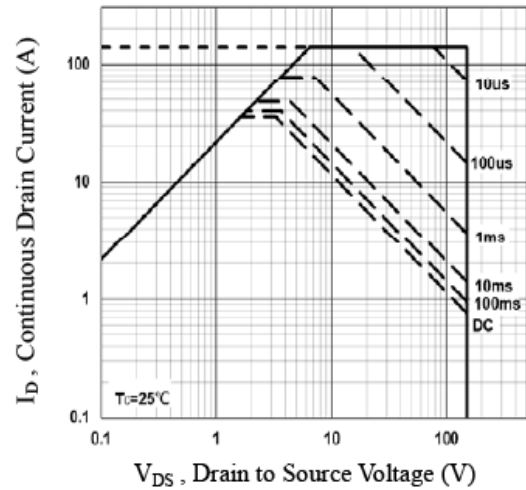
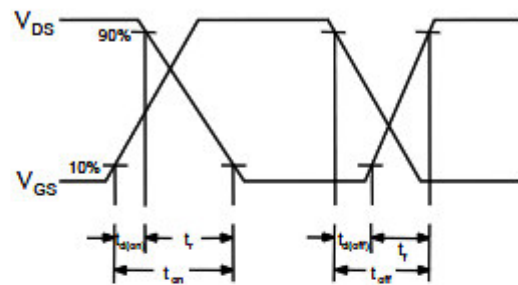
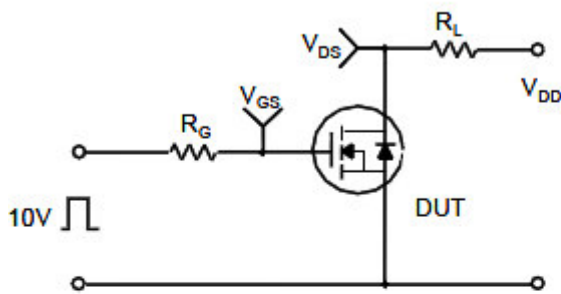
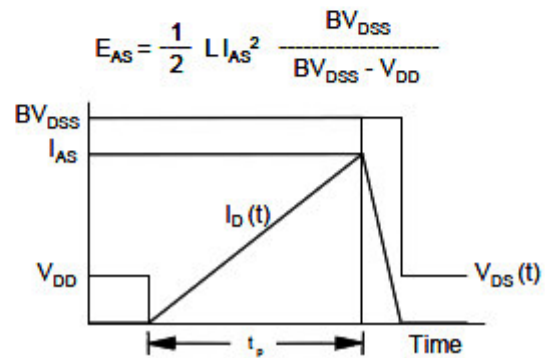
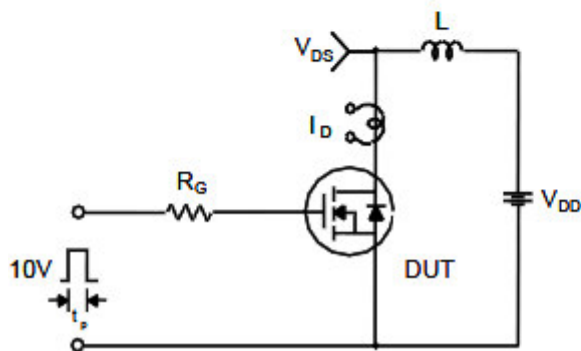


Fig.8 Maximum Safe Operation Area

Resistive Switching Test Circuit & Waveforms

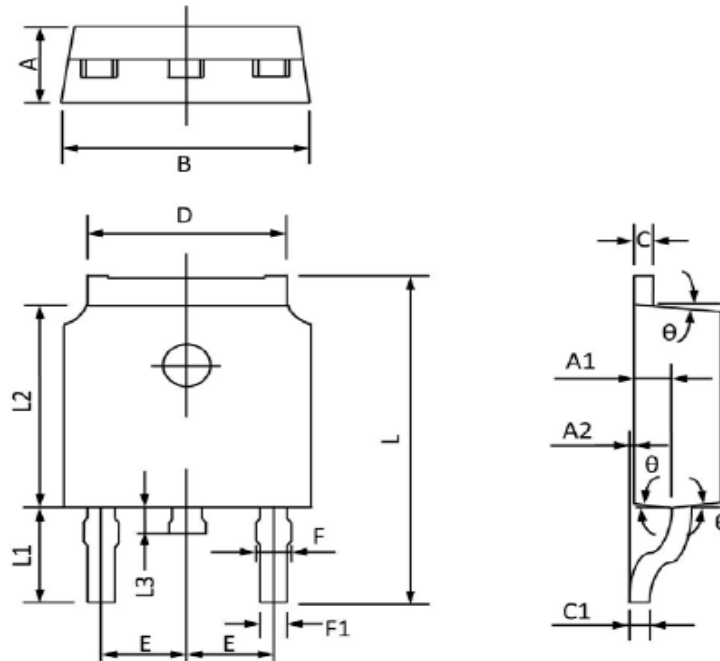


Unclamped Inductive Switching Test Circuit & Waveforms



Package Dimension

TO-252-2L










Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.20	2.40	0.087	0.094
A1	0.91	1.11	0.036	0.044
A2	0.00	0.15	0.000	0.006
B	6.40	6.80	0.252	0.268
C	0.46	0.58	0.018	0.023
C1	0.46	0.58	0.018	0.023
D	5.10	5.50	0.201	0.217
E	2.186	2.386	0.086	0.094
F	0.60	0.94	0.024	0.037
F1	0.50	0.86	0.020	0.034
L	9.40	10.40	0.370	0.409
L1	2.40	3.00	0.094	0.118
L2	5.40	6.20	0.213	0.244
L3	0.60	1.20	0.024	0.047
θ	3°	9°	3°	9°



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