GSM6184DF

60V N-Channel Enhancement Mode MOSFET

Product Description

The N-Channel enhancement mode power field effect transistor is using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

The device is well suited for high efficiency fast switching applications.
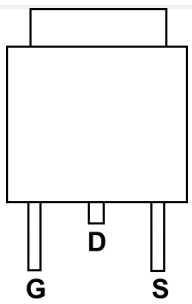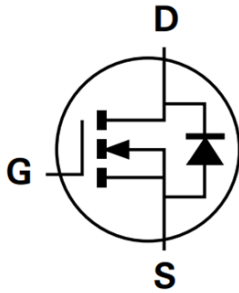
Features

- $R_{DS(ON)}=92m\Omega@V_{GS}=10V$
- $R_{DS(ON)}=100m\Omega@V_{GS}=4.5V$
- Improved dv/dt capability
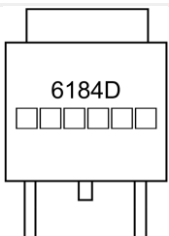- Fast switching
- 100% EAS guaranteed.

Applications

- Motor Drive
- Power Tools
- LED Lighting

Packages & Pin Assignments

GSM6184DF (TO-252)	Equivalent Circuit

Pin	Description
1	Gate
2	Drian
3	Source

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Ordering and Marking Information

Ordering Information			
Part Number	**Package**	**Part Marking**	**Quantity / Reel**
GSM6184DF	TO-252	6184D ▢▢▢▢▢▢	2,500 PCS

GSM6184 [1] [2]

- **Product Code:**
  GSM6184

- **Package Code:**
  [1] is **D** for TO-252

- **Green Level:**
  [2] is **F** for RoHS Compliant
  and Halogen Free

Marking Information

6184D ▢▢▢▢▢

- **Product Code:**
  6184D

- **GS Code:**
  ▢▢▢▢▢▢

Absolute Maximum Ratings

T_A=25ºC, unless otherwise specified

Symbol	Parameter		Value	Unit
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current[1]	T_C=25ºC	10	A
		T_C=100ºC	6	
		T_A=25ºC	3	
		T_A=70ºC	2	
I_{DM}	Pulsed Drain Current[2]		20	A
I_{AS}	Single Pulse Avalanche Current		11.2	A
E_{AS}	Single Pulse Avalanche Energy[3]		6.3	mJ
P_D	Total Power Dissipation[4]	T_C=25ºC	20.8	W
		T_C=100ºC	8.3	
		T_A=25ºC	2	
		T_A=70ºC	1.2	
T_J	Operating Junction Temperature		-55 to +150	ºC
T_{STG}	Storage Temperature Range		-55 to +150	ºC
$R_{\theta JC}$	Thermal Resistance, Junction to Case[1]		6	ºC/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient[1]		62	ºC/W

Electrical Characteristics

T_A=25ºC, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V	-	-	1	uA
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	-	3	V
$R_{DS(ON)}$	Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=6A	-	85	92	mΩ
		V_{GS}=4.5V, I_D=3A	-	90	100	
g_{FS}	Forward Transconductance	V_{DS}=10V, I_D=3A	-	3.6	-	S
Dynamic characteristics						
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz	-	511	-	pF
C_{oss}	Output Capacitance		-	38	-	
C_{rss}	Reverse Transfer Capacitance		-	25	-	
Q_g	Total Gate Charge	V_{DS}=48V, V_{GS}=4.5V, I_D=10A	-	4.9	-	nC
Q_{gs}	Gate-Source Charge		-	1.8	-	
Q_{gd}	Gate-Drain Charge		-	2.2	-	
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=30V, I_D=3A, V_{GS}=4.5V, R_G=3.3Ω	-	6	-	ns
t_r	Turn-On Rise Time		-	9	-	
$t_{d(off)}$	Turn-Off Delay Time		-	18	-	
t_f	Turn-Off Fall Time		-	5	-	
Diode characteristics						
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V, I_S=10A	-	-	1.4	V
I_S	Continuous Source Current[1]	V_G=V_D=0V, Force Current	-	-	10	A
trr	Reverse Recovery Time	I_S=3A, V_{GS}=0V dI/dt=100A/μs	-	19	-	ns
Qrr	Reverse Recovery Charge		-	28	-	nC

Note:
1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%
3. The E_{AS} data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=11.2A
4. The power dissipation is limited by 150℃ junction temperature
5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

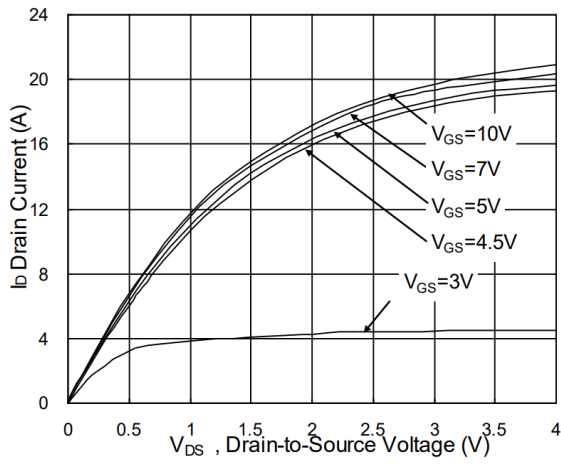## Typical Performance Characteristics

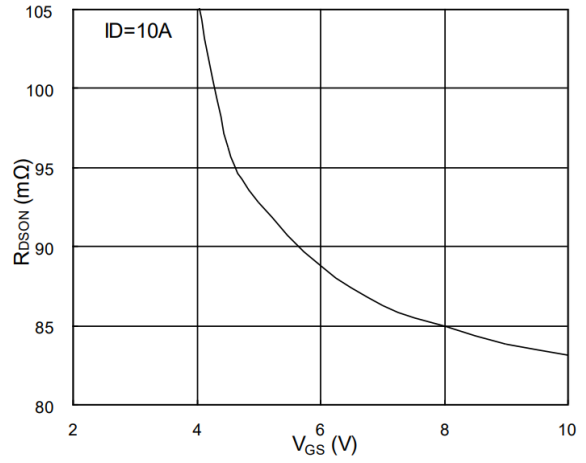Fig 1. Output Characteristics

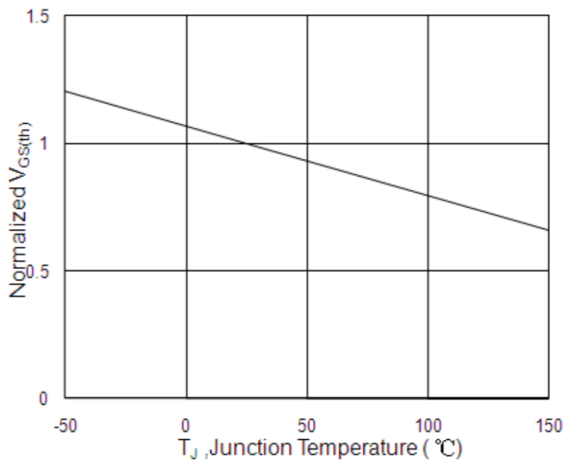Fig. 2 On-Resistance vs. Gate Source
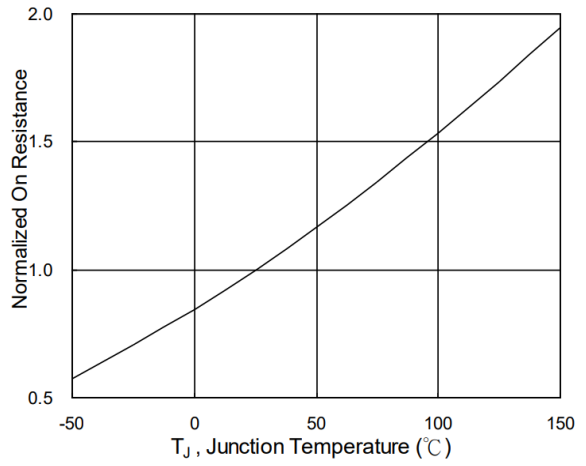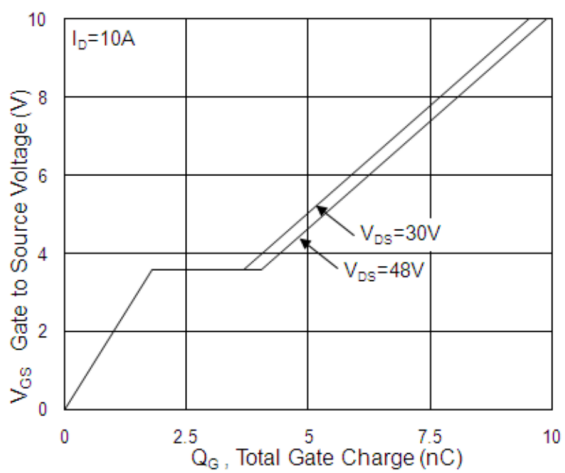

Fig. 3 Normalized Gate Threshold Voltage

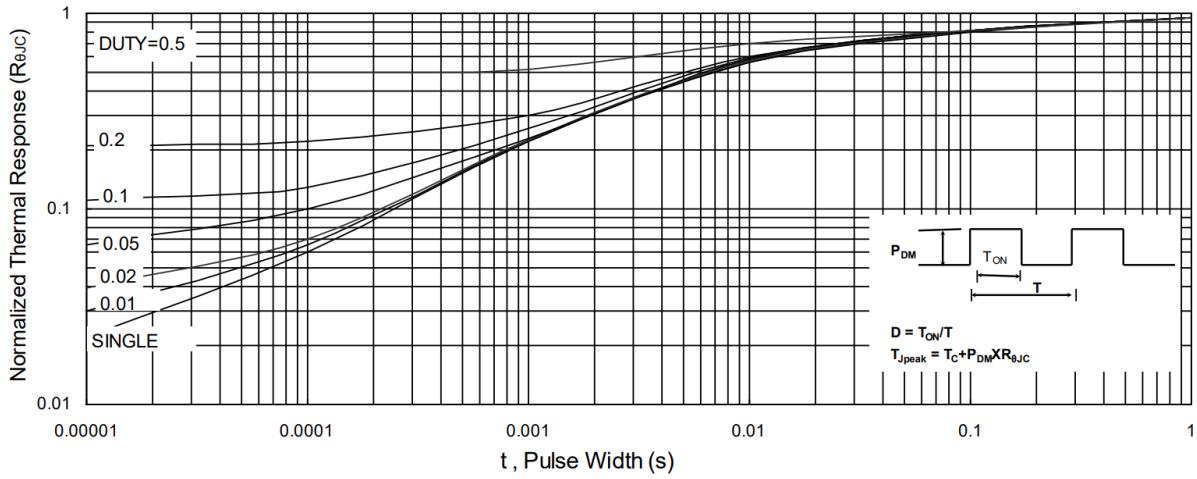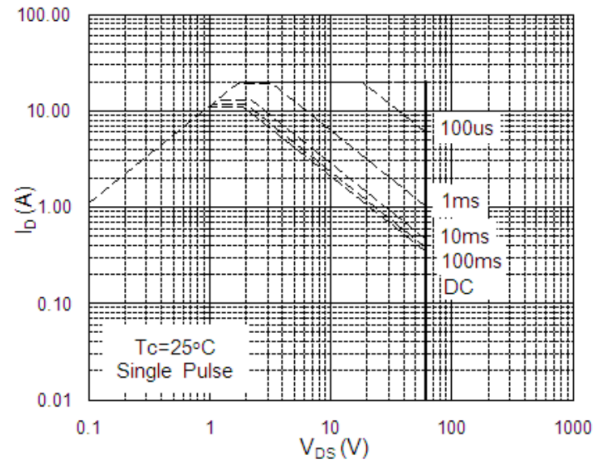Fig. 4 Normalized On-Resistance

Fig. 5 Gate Charge Characteristics
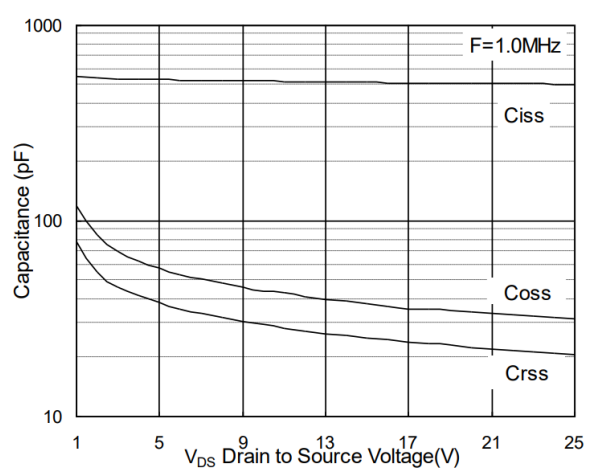
Fig. 6 Typical Capacitance

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Typical Performance Characteristics

Fig. 7 Diode Forward Characteristics

Fig. 8 Safe Operating Area

$$D = T_{ON}/T$$
$$T_{Jpeak} = T_C + P_{DM} X R_{\theta JC}$$

Fig. 9 Transient Thermal Impedance
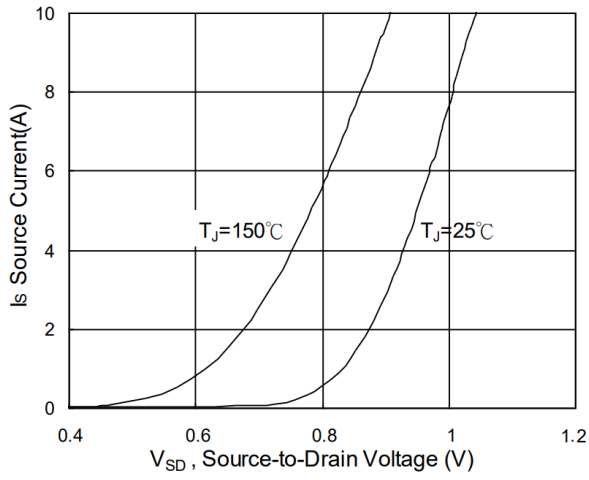
TO-252

Package Dimension

BACKSIDE VIEW

GAUGE PLANE
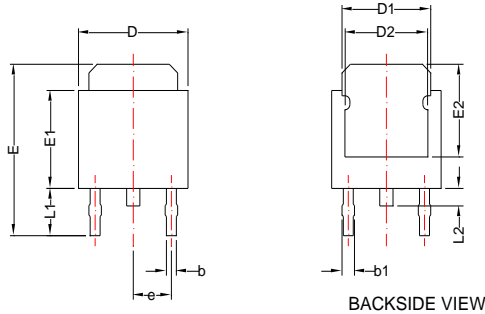
Recommended Land Pattern
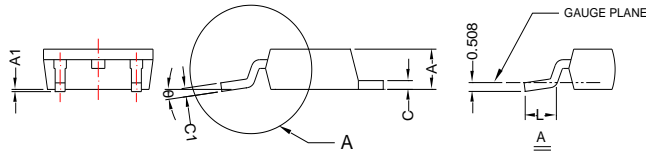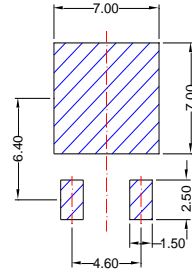
Dimensions				
Symbol	**Millimeters**		**Inches**	
	MIN	**MAX**	**MIN**	**MAX**
A	2.18	2.40	0.086	0.094
A1	0.00	0.15	0.000	0.006
b	0.50	0.90	0.020	0.035
c	0.45	0.89	0.018	0.035
c1	0.40	0.61	0.016	0.024
D	6.35	6.80	0.250	0.268
D1	4.95	5.50	0.195	0.217
D2	3.81	-	0.150	-
E	9.40	10.41	0.370	0.410
E1	5.33	5.80	0.210	0.228
E2	4.57	-	0.180	-
e	2.286 BSC		0.090 BSC	
L	1.40	1.78	0.055	0.070
L1	2.4	3.00	0.094	0.118
θ	0°	8°	0°	8°

NOTE:

Dimensions are exclusive of Burrs, Mold Flash & Tie Bar extrusions.

GSM6184DF

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CONTACT US

GS Headquarter	
🗑	4F., No.43-1, Lane11, Sec.6, Minquan E.Rd Neihu District Taipei City 114, Taiwan (R.O.C)
☎	886-2-2657-9980
📠	886-2-2657-3630
✉@	sales_twn@gs-power.com

RD Division	
🗑	824 Bolton Drive Milpitas. CA. 95035
☎	1-408-457-0587

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