

GSM3335SF

30V P-Channel Enhancement Mode MOSFET

Product Description

The P-Channel enhancement mode power field effect transistor is using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

This device is well suited for high efficiency fast switching applications.

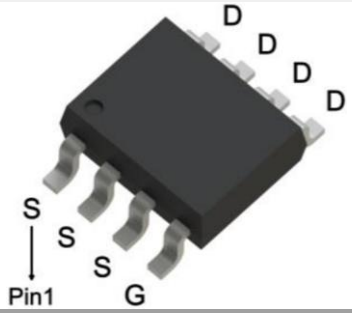
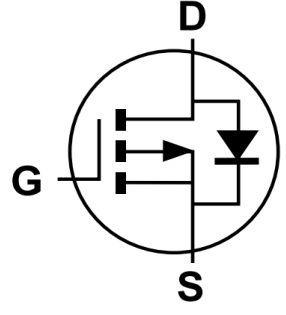
Features

- $R_{DS(ON)}=5m\Omega@V_{GS}=-10V$
- $R_{DS(ON)}=7.8m\Omega@V_{GS}=-4.5V$
- Fast switching
- Suit for -4.5V Gate Drive Applications
- Green Device Available

Applications

- Motor Driver Applications
- POL Applications
- Load Switch
- LED Application

Packages & Pin Assignments

GSM3335SF (SOP-8)		Equivalent Circuit
		
Pin	Description	
1	Source	
2	Source	
3	Source	
4	Gate	
5	Drain	
6	Drain	
7	Drain	
8	Drain	

Ordering and Marking Information

Ordering Information			
Part Number	Package	Part Marking	Quantity / Reel
GSM3335SF	SOP-8	3335SF □□□□□□	4,000 PCS
GSM3335 1 2			
- Product Code: GSM3335 - Package Code: 1 is S for SOP-8 - Green Level: 2 is F for RoHS Compliant and Halogen Free			
Marking Information			
 - Package Code: 3335SF - GS Code: □□□□□□			

Absolute Maximum Ratings

T_A=25°C, unless otherwise specified

Symbol	Parameter	Value	Unit
V _{DS}	Drain-Source Voltage	-30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D	Continuous Drain Current	T _A =25°C	A
		T _A =70°C	
I _{DM}	Pulsed Drain Current	-100	A
P _D	Power Dissipation	T _A =25°C	W
		T _A =70°C	
T _J	Operating Junction Temperature Range	-55 to +150	°C
T _{STG}	Storage Temperature Range	-55 to +150	°C
R _{θJA}	Thermal Resistance, Junction to Ambient (t ≤ 10s)	40	°C/W
	Thermal Resistance, Junction to Ambient (Steady State)	75	°C/W
R _{θJC}	Thermal Resistance, Junction to Case	24	°C/W

Electrical Characteristics

T_A=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1.2	-	-2.5	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±25V	-	-	±100	nA
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-30V, V _{GS} =0V	-	-	-1	uA
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =-1A	-	-	-1	V
R _{DS(ON)}	Drain-Source On-Resistance	V _{GS} =-10V, I _D =-20A	-	4.5	5	mΩ
		V _{GS} =-4.5V, I _D =-10A	-	6.3	7.8	
Gate charge characteristics						
Q _g	Total Gate Charge	V _{DD} =-15V, V _{GS} =10V, I _D =-10A	-	150	-	nC
Q _{gs}	Gate-Source Charge		-	24	-	
Q _{gd}	Gate-Drain Charge		-	28	-	
Dynamic characteristics						
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	-	7500	-	pF
C _{oss}	Output Capacitance		-	1200	-	
C _{rss}	Reverse Transfer Capacitance		-	940	-	
t _{d(on)}	Turn-On Time	V _{DS} =-15V, V _{GS} =-10V, R _g =6Ω, I _{DS} =-1A	-	25	-	ns
t _r	Rise Time		-	35	-	
t _{d(off)}	Turn-Off Time		-	100	-	
t _f	Fall Time		-	50	-	

Typical Performance Characteristics

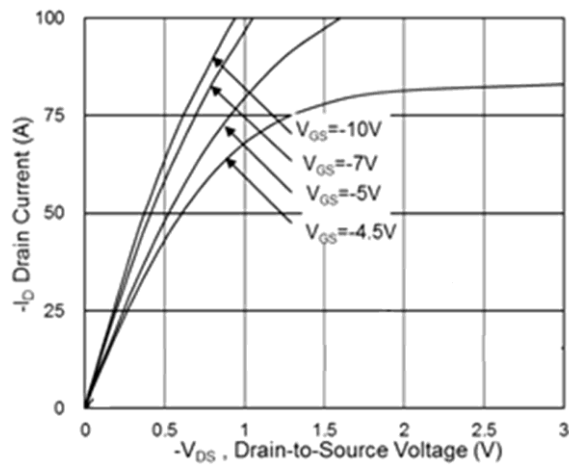


Figure 1. Output Characteristics

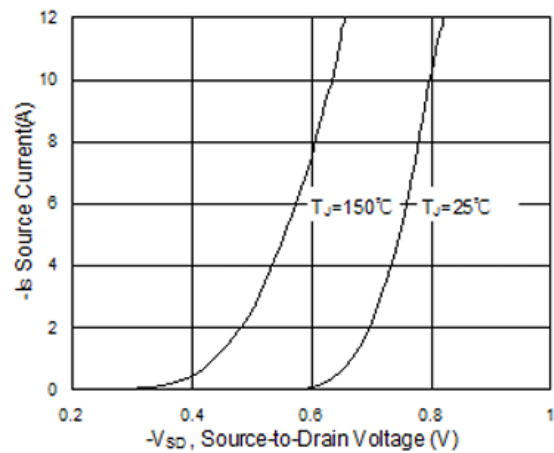


Figure 2. Forward Characteristics of Reverse

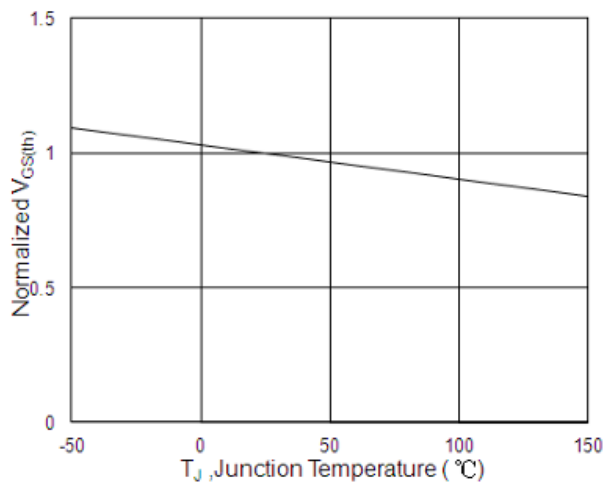


Figure 3. Normalized $V_{GS(th)}$ vs. T_J

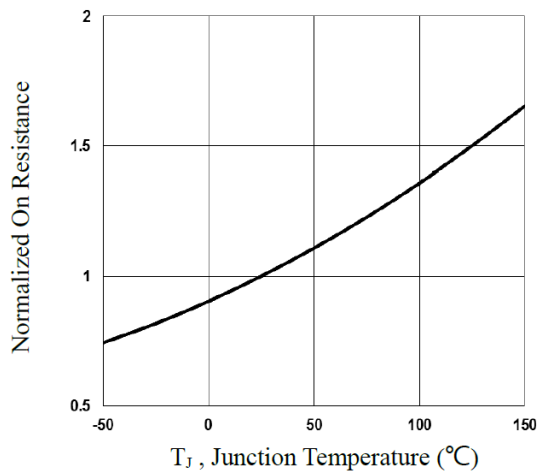


Figure 4. Normalized $R_{DS(on)}$ vs. T_J

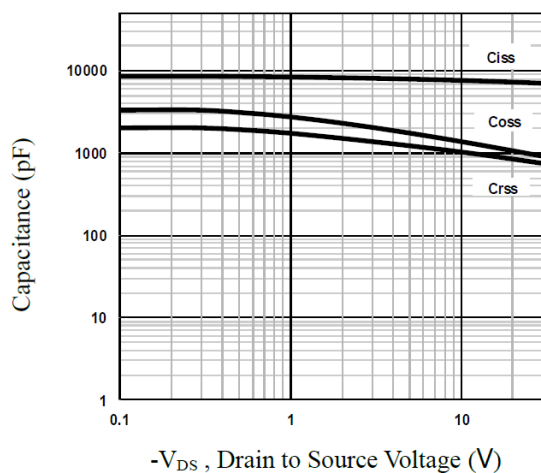


Figure 5. Capacitance

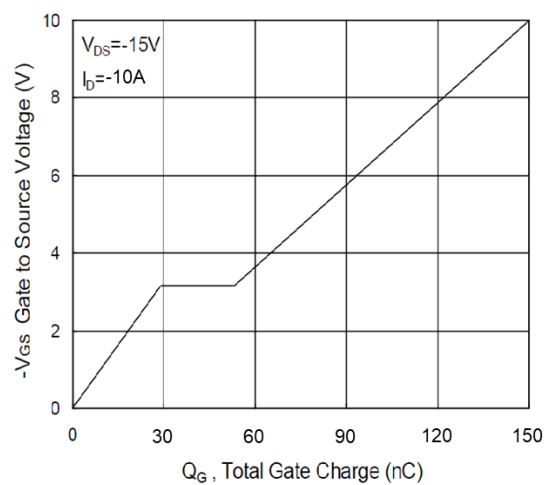


Figure 6. Gate Charge

Typical Performance Characteristics

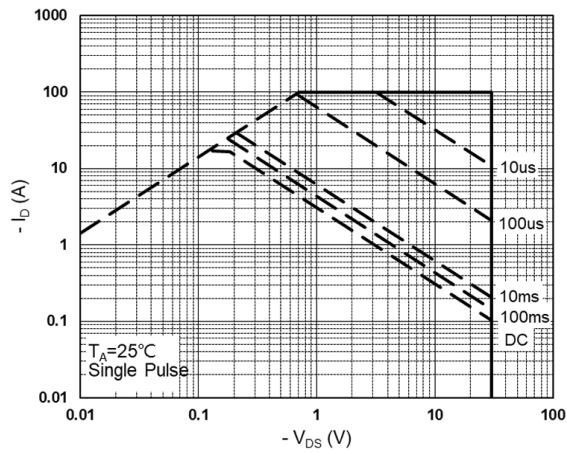


Figure 7. Maximum Safe Operating Area

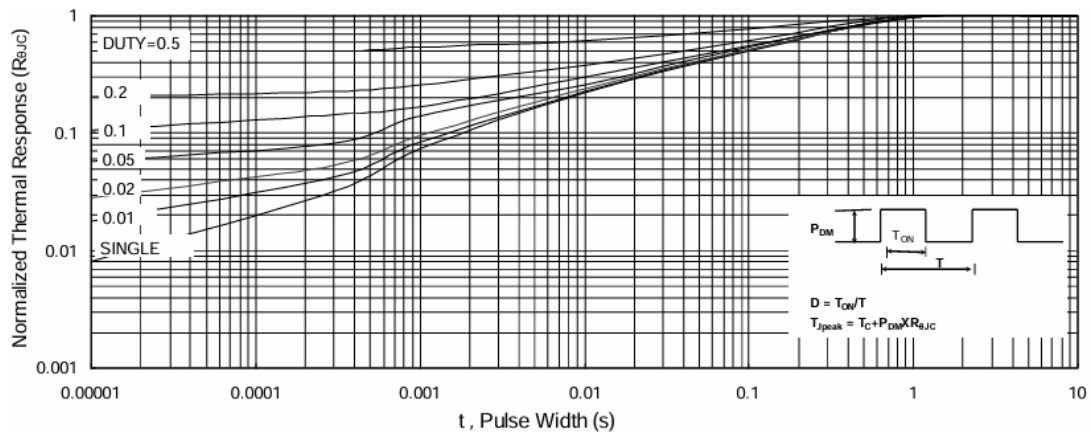
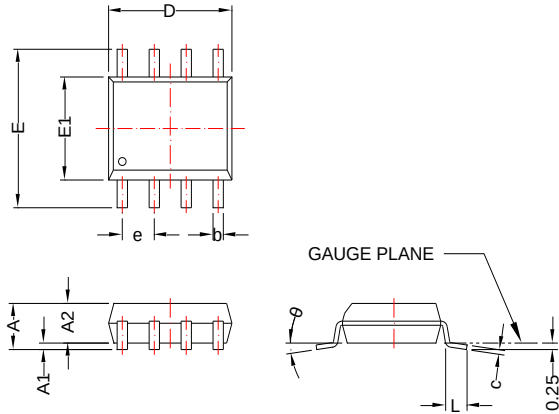


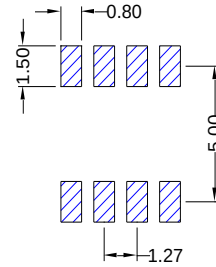
Figure 8. Normalized Transient Thermal Resistance

SOP-8

Package Dimension



Recommended Land Pattern



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.75	-	0.069
A1	0.10	0.15	0.004	0.006
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.10	0.25	0.004	0.010
D	4.70	5.10	0.185	0.201
D1	1.50	-	0.059	-
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	1.00	-	0.039	-
e	1.27 BSC		0.050 BSC	
L	0.4	1.27	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

Dimensions are exclusive of Burrs, Mold Flash & Tie Bar extrusions.

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CONTACT US

GS Headquarter	
	4F.,No.43-1,Lane11,Sec.6,Minquan E.Rd NeiHu District Taipei City 114, Taiwan (R.O.C)
	886-2-2657-9980
	886-2-2657-3630
	sales_twn@gs-power.com

RD Division	
	824 Bolton Drive Milpitas. CA. 95035
	1-408-457-0587