

# GSM3106ZF

## 30V N-Channel MOSFETs

### Product Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

### Features

- 30V, 54A,  $R_{DS(ON)}=6m\Omega@V_{GS}=10V$
- High Power and current handling capability
- Lead Free and Green Devices Available
- DFN3x3-8L package design

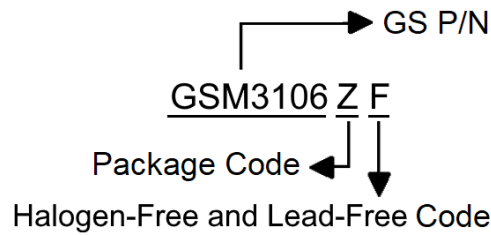
### Applications

- MB / VGA / Vcore
- POL Applications
- SMPS 2nd SR

### Packages & Pin Assignments

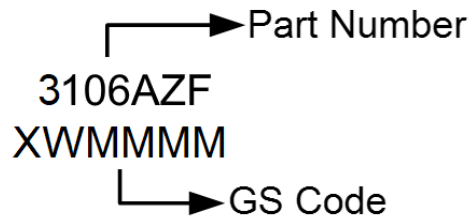
GSM3106ZF (DFN3x3-8L)	
<p style="text-align: center;">Top View</p>	
Pin	Description
1	Source
2	Source
3	Source
4	Gate
5	Drain
6	Drain
7	Drain
8	Drain

## Ordering Information



Part Number	Package	Quantity
GSM3106ZF	DFN3x3-8L	5000pcs

## Marking Information



## Absolute Maximum Ratings

$T_A=25^{\circ}\text{C}$  Unless otherwise noted

Symbol	Parameter	Typical	Unit
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_C=25^{\circ}\text{C}^1$	54
		$T_C=70^{\circ}\text{C}$	43
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	80	A
$E_{AS}$	Single Pulse Avalanche Energy <sup>3</sup>	25	mJ
$P_D$	Power Dissipation $T_C=25^{\circ}\text{C}$	26.6	W
	Power Dissipation $T_C=70^{\circ}\text{C}$	17.1	W
$T_J$	Operating Junction Temperature Range	-55 to +150	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to +150	$^{\circ}\text{C}$
$R_{\theta JC}$	Thermal Resistance-Junction to Case	4.7	$^{\circ}\text{C}/\text{W}$

Note :

1. The maximum current rating is package limited..
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3.  $E_{AS}$  condition:  $T_J=25^{\circ}\text{C}$ ,  $V_{DS}=30\text{V}$ ,  $V_{GS}=10\text{V}$ ,  $R_G=25\Omega$ ,  $L=0.5\text{mH}$ ,  $I_{peak}=24\text{A}$ .

## Electrical Characteristics

T<sub>A</sub>=25°C Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1.0		2.5	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V			1	uA
V <sub>SD</sub>	Diode Forward Voltage <sup>3</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =2A			1	V
R <sub>DS(on)</sub>	Drain-Source On-Resistance <sup>3</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		4.8	6	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A		6.9	9	
<b>Gate charge characteristics</b>						
Q <sub>g</sub>	Total Gate Charge <sup>3,4</sup>	V <sub>DD</sub> =15V, I <sub>D</sub> =9A		16.7		nC
Q <sub>gs</sub>	Gate-Source Charge <sup>3,4</sup>			2.2		
Q <sub>gd</sub>	Gate-Drain Charge <sup>3,4</sup>			3.5		
<b>Dynamic characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1.0MHz		1155		pF
C <sub>oss</sub>	Output Capacitance			456		
C <sub>rss</sub>	Reverse Transfer Capacitance			72		
t <sub>d(on)</sub>	Turn-On Time	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, R <sub>g</sub> =3Ω, I <sub>D</sub> =9A		3.5		ns
t <sub>r</sub>	Rise Time			5.5		
t <sub>d(off)</sub>	Turn-Off Time			13.5		
t <sub>f</sub>	Fall Time			4.6		

## Typical Performance Characteristics

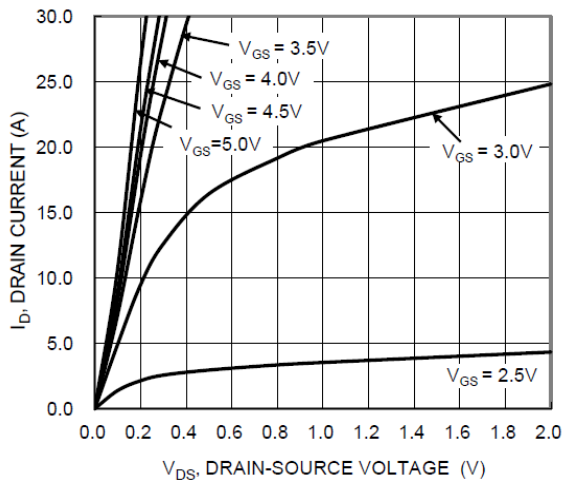


Figure 1. Output Characteristics

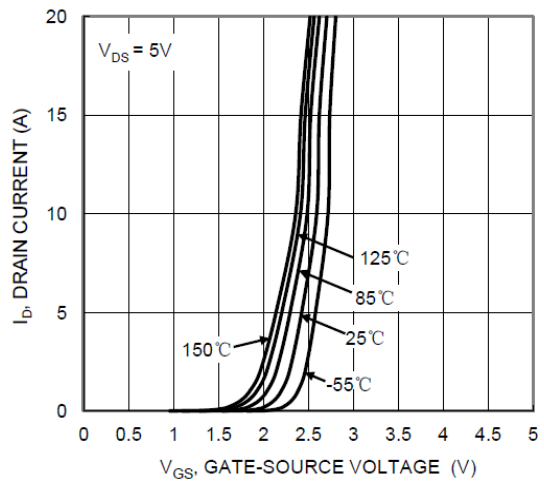


Figure 2. Transfer Characteristics

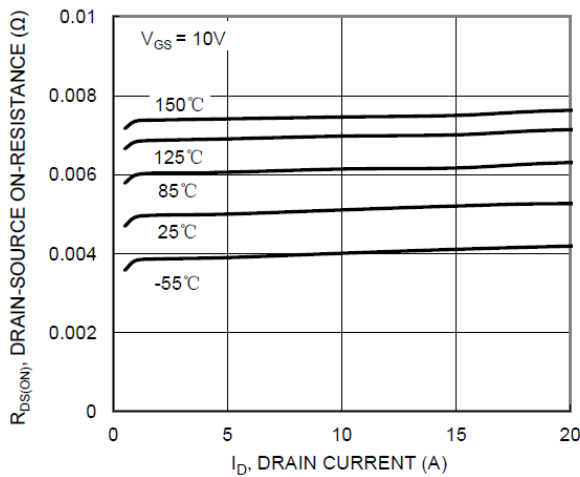


Figure 3. On-Resistance vs. Drain Current

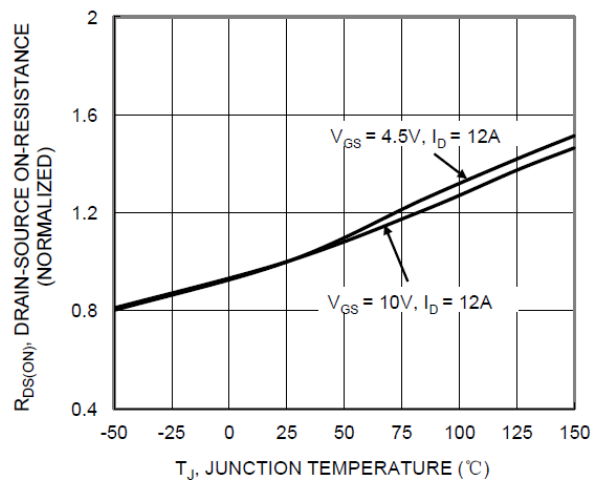


Figure 4. Normalized  $R_{DS(on)}$  vs.  $T_J$

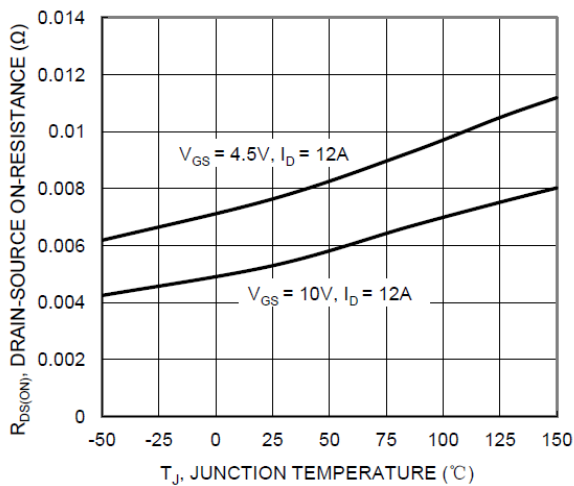


Figure 5. On-Resistance Variation with Temperature

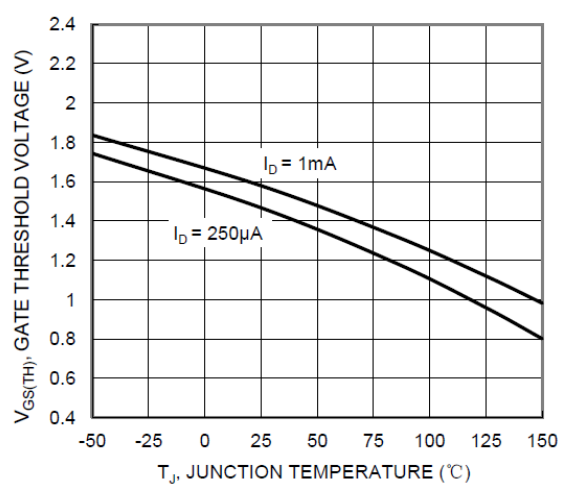


Figure 6. Gate Threshold Variation vs.  $T_J$

## Typical Performance Characteristics (Continue)

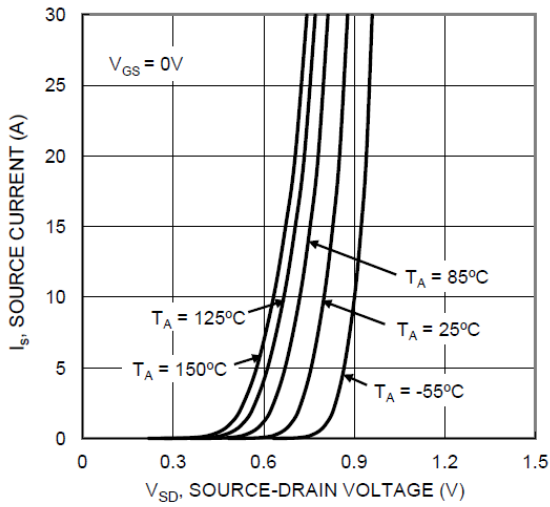


Figure 7. Diode Forward Voltage vs. Current

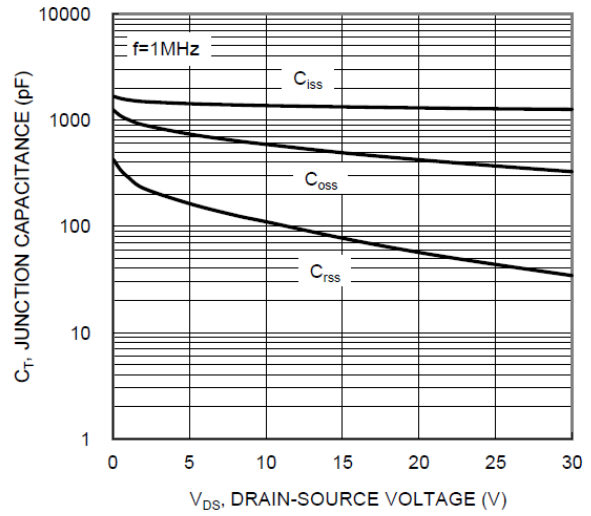


Figure 8. Capacitance

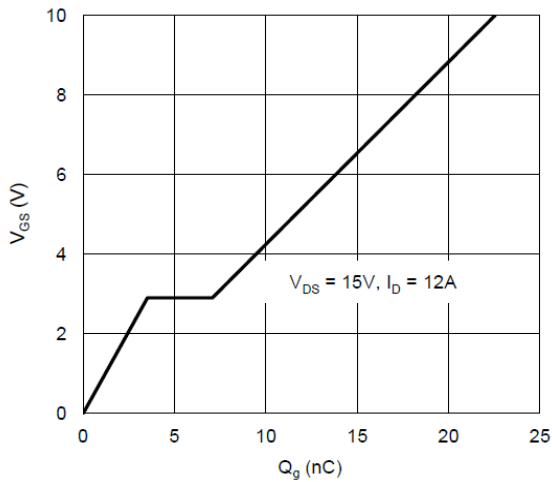


Figure 9. Gate Charge Waveform

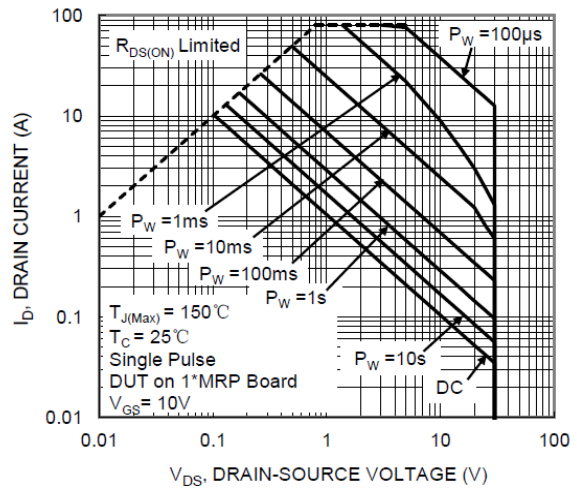


Figure 10. Maximum Safe Operating Area

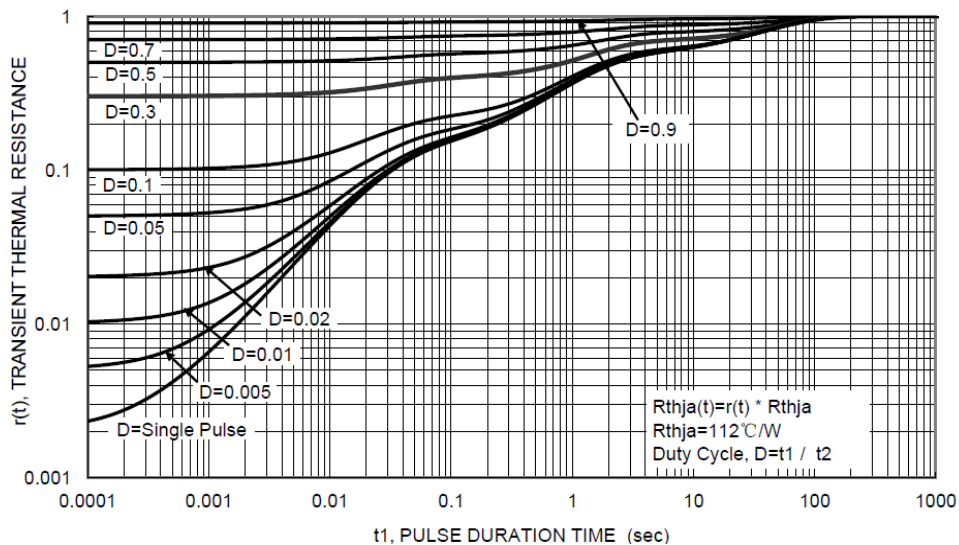
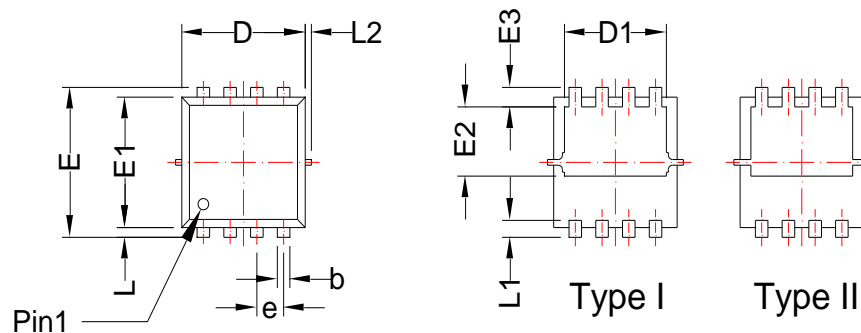


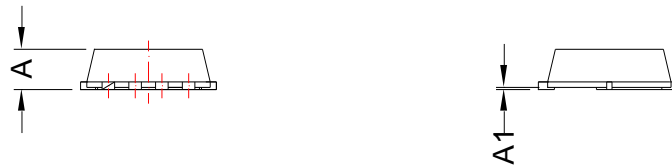
Figure 11. Normalized Transient Thermal Resistance

## Package Dimension

### DFN3X3-8L



BACKSIDE VIEW



DIMENSION D AND E1 DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.5mm PER INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.5mm PER SIDE.

Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.70	0.90	0.028	0.035
A1	0.00	0.05	0.000	0.002
b	0.24	0.37	0.009	0.015
c	0.10	0.25	0.004	0.010
D	2.90	3.25	0.114	0.128
D1	2.35	2.60	0.093	0.102
E	3.05	3.45	0.120	0.136
E1	2.90	3.20	0.114	0.126
E2	1.35	2.00	0.053	0.079
E3	0.30	0.60	0.012	0.024
e	0.65 BSC		0.026 BSC	
L	0.02	0.2	0.001	0.008
L1	0.28	0.5	0.011	0.020
L2	---	0.15	---	0.006





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## CONTACT US

GS Headquarter	
	4F.,No.43-1,Lane11,Sec.6,Minquan E.Rd Neihu District Taipei City 114, Taiwan (R.O.C)
	886-2-2657-9980
	886-2-2657-3630
	sales_twn@gs-power.com

RD Division	
	824 Bolton Drive Milpitas. CA. 95035
	1-408-457-0587