GSM1151SF

100V P-Channel Enhancement Mode MOSFET

Product Description

The P-Channel enhancement mode power field effect transistor is using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

This device is well suited for high efficiency fast switching applications.

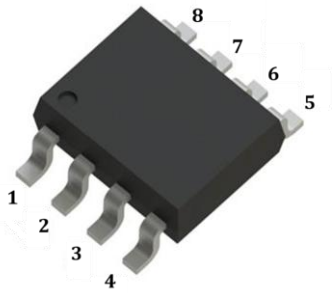
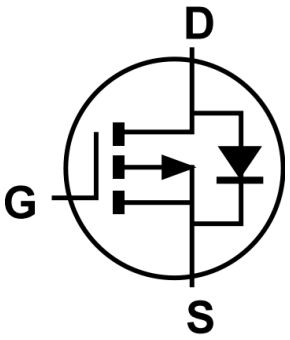
Features

- $R_{DS(ON)}$ =50mΩ@V_{GS}= -10V
- $R_{DS(ON)}$ =60mΩ@V_{GS}= -4.5V
- SOP-8 Package
- RoHS Compliant and Halogen Free

Applications

- Networking
- Load Switch
- LED applications

Packages & Pin Assignments

GSM1151SF (SOP-8)	Equivalent Circuit
	

Pin	Description
1	Source
2	Source
3	Source
4	Gate
5	Drain
6	Drain
7	Drain
8	Drain

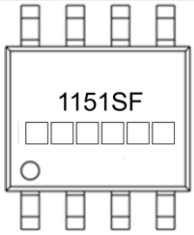
Ordering and Marking Information

Ordering Information			
Part Number	**Package**	**Part Marking**	**Quantity / Reel**
GSM1151SF	SOP-8	1151SF □□□□□□	4,000 PCS

GSM1151 1 2

- **Product Code:** GSM1151
- **Package Code:** 1 is **S** for SOP-8
- **Green Level:** 2 is **F** for RoHS Compliant and Halogen Free

Marking Information



- **Product Code:** 1151SF
- **GS Code:** □□□□□□

Absolute Maximum Ratings

T_A=25ºC, unless otherwise specified

Symbol	Parameter		Value	Unit
V_{DSS}	Drain-Source Voltage		-100	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current [1]	T_A=25ºC	-4.5	A
		T_A=70ºC	-3.6	
I_{DM}	Pulsed Drain Current [2]		-18	A
I_{AS}	Single Pulse Avalanche Current, L = 0.5mH [3]		-16	A
E_{AS}	Single Pulse Avalanche Energy, L = 0.5mH [3]		85	mJ
P_D	Power Dissipation [4]	T_A=25ºC	1.8	W
		T_A=70ºC	1.1	
T_J	Operating Junction Temperature Range		-55 to +150	ºC
T_{STG}	Storage Temperature Range		-55 to +150	ºC
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [1]		70	ºC/W

Electrical Characteristics

TA=25ºC, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-100	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1.2	-	-2.5	V
I_{GSS}	Gate-Source Leakage Current	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-100V, V_{GS}=0V	-	-	-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance [2]	V_{GS}=-10V, I_D=-10A	-	42	50	mΩ
		V_{GS}=-4.5V, I_D=-8A	-	46	60	
g_{FS}	Forward Transconductance	V_{DS}=-10V, I_D=-10A	-	26	-	S
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_S=-1A	-	-	-1	V
Dynamic characteristics						
C_{iss}	Input Capacitance	V_{DS}=-25V, V_{GS}=0V, f=1MHz	-	6516	-	pF
C_{oss}	Output Capacitance		-	223	-	
C_{rss}	Reverse Transfer Capacitance		-	125	-	
Q_g	Total Gate Charge	V_{DS}=-80V, V_{GS}=-10V, I_D=-14A	-	92	-	nC
Q_{gs}	Gate-Source Charge		-	17.5	-	
Q_{gd}	Gate-Drain Charge		-	14	-	
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-50V, V_{GS}=-10V, Rg=3.3Ω, I_D=-14A	-	20.5	-	ns
t_r	Turn-On Rise Time		-	32.2	-	
$t_{d(off)}$	Turn-Off Delay Time		-	123	-	
t_f	Turn-Off Fall Time		-	63.7	-	

Note:

1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2_{OZ} copper.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3. The E_{AS} data shows Max. rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.5mH, I_{AS}=-16A
4. The power dissipation is limited by 150℃ junction temperature

Typical Performance Characteristics

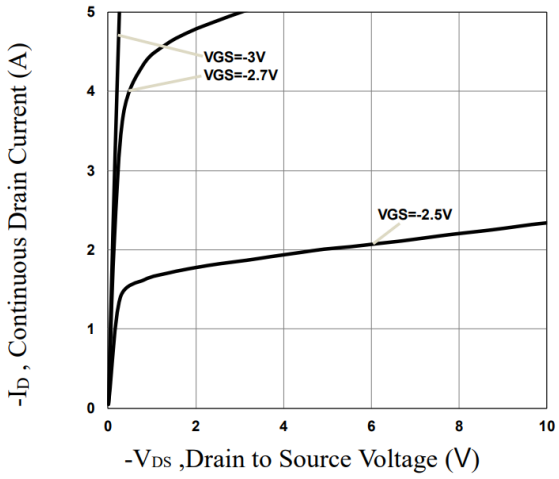


Fig.1 Typical Output Characteristics

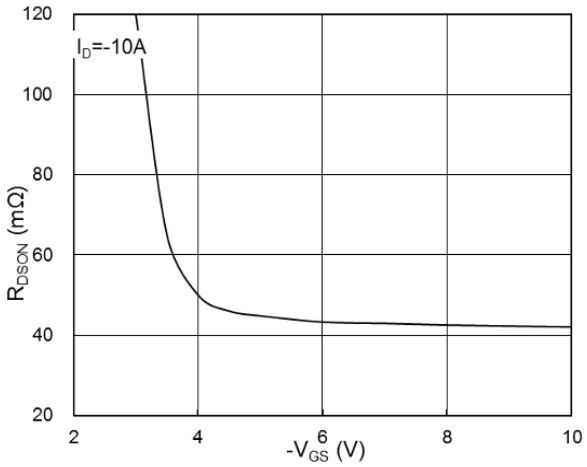


Fig.2 On-Resistance vs V_{GS}

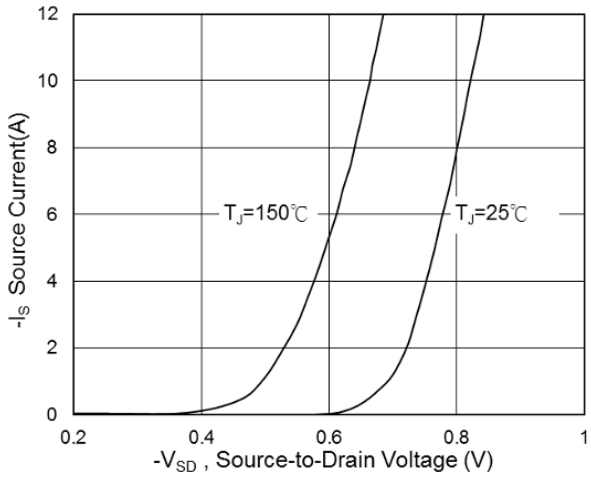


Fig.3 Typical V_{SD} Diode Forward Voltage

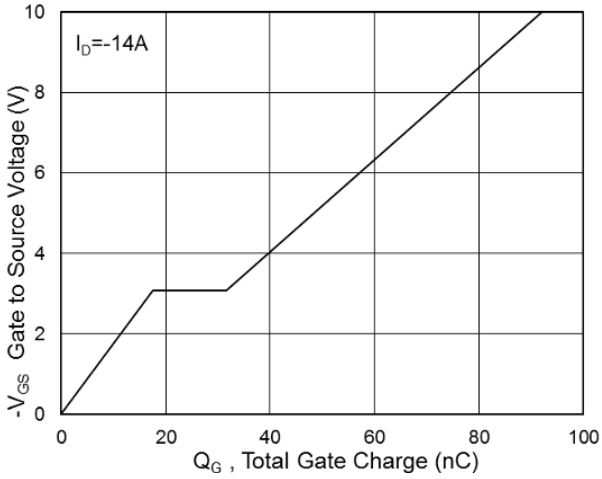


Fig.4 Gate-Charge Characteristics

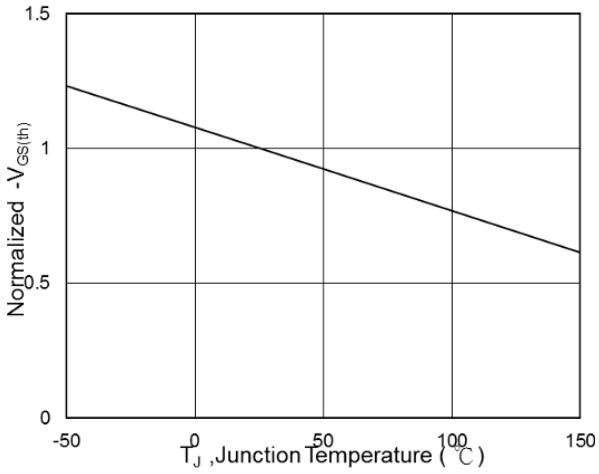


Fig.5 Normalized $V_{GS(th)}$ vs T_J

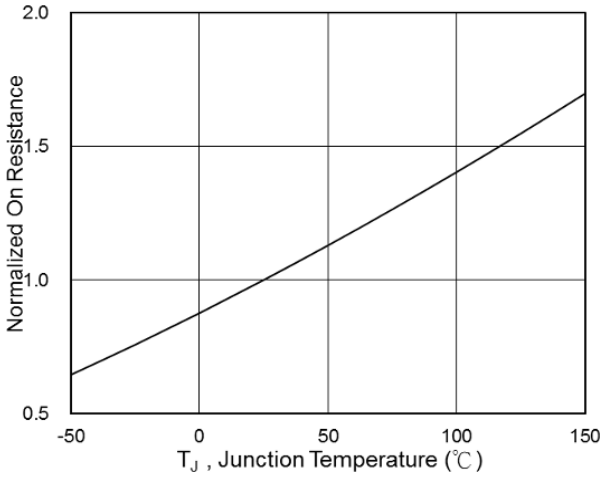


Fig.6 Normalized $R_{DS(ON)}$ vs T_J

Typical Performance Characteristics

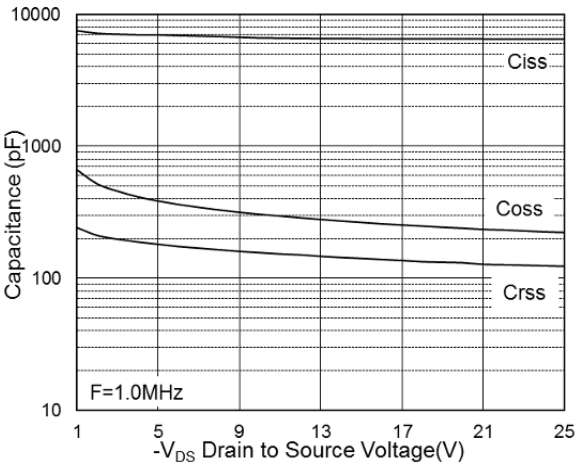


Fig.7 Capacitance

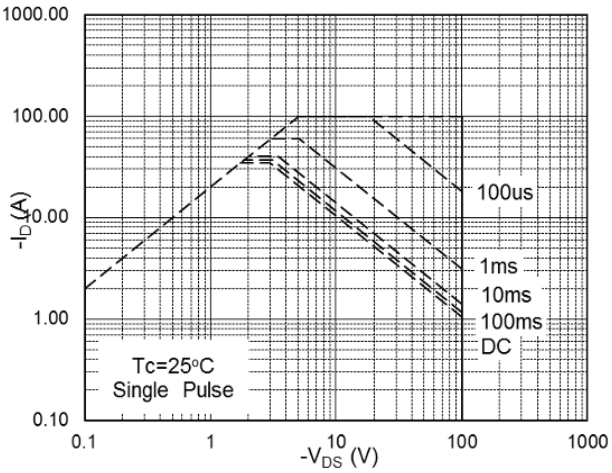


Fig.8 Safe Operating Area (SOA)

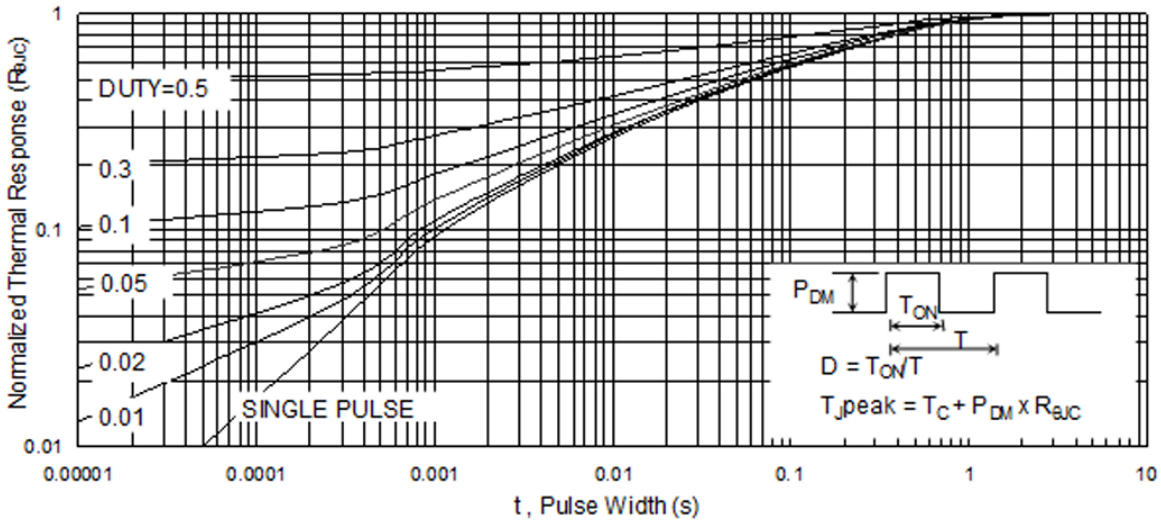
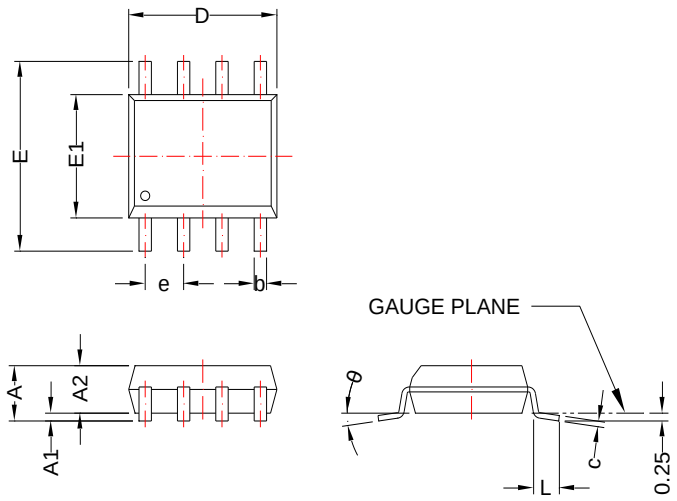


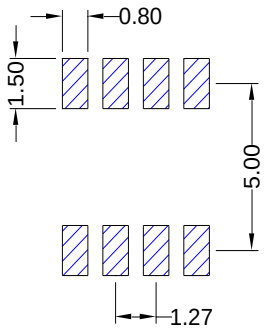
Fig.9 Normalized Maximum Transient Thermal Impedance

SOP-8

Package Dimension



Recommended Land Pattern



Dimensions

Symbol	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.10	0.25	0.004	0.010
D	4.70	5.10	0.185	0.201
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.4	1.27	0.016	0.050
θ	0°	8°	0°	8°

NOTE:
Dimensions are exclusive of Burrs, Mold Flash & Tie Bar extrusions.

NOTICE

- Globaltech Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all Globaltech Semiconductor products described or contained herein. Globaltech Semiconductor products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

- Applications shown on the herein document are examples of standard use and operation. Customers are responsible in comprehending the suitable use in particular applications. Globaltech Semiconductor makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

- The information furnished is believed to be accurate and reliable. However, Globaltech Semiconductor assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Globaltech Semiconductor. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information without express written approval of Globaltech Semiconductor.

CONTACT US

GS Headquarter	
	4F.,No.43-1,Lane11,Sec.6,Minquan E.Rd Neihu District Taipei City 114, Taiwan (R.O.C)
	886-2-2657-9980
	886-2-2657-3630
	sales_twn@gs-power.com

RD Division	
	824 Bolton Drive Milpitas. CA. 95035
	1-408-457-0587