GS5484

21V, 3A, 340KHz Synchronous Step-Down DC/DC Converter

Product Description

The GS5484 is a synchronous step-down DC/DC converter that provides wide 5V to 21V input voltage range and 3A continuous load current capability.

Other features such as integrated Boot-Diode, programmable Soft-Start, total fault-free protection and 94% conversion efficiency at 5V/2A output make GS5484 ideally to be used in portable consumer electronics.

The GS5484 is available in an 8-pin SOIC package, provides a very compact system solution and good thermal conductance.

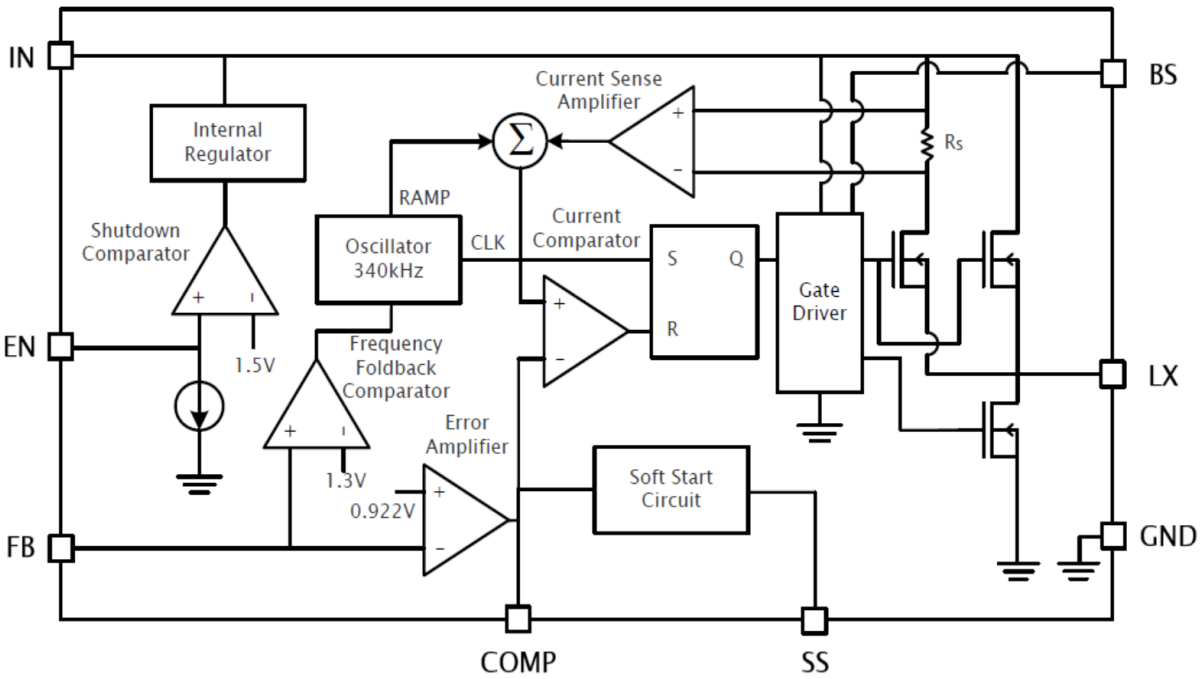
Features

- Wide Input Voltage from 5V to 21V
- 3A Output Current
- Adjustable Output Voltage from 0.922V to 15V
- 90/80mΩ integrated Power MOSFET
- High Efficiency Up to 94% at 5V/2A Output
- Fixed 340KHz Switching Frequency.
- Current Mode PWM Operation
- Soft-Start Function
- Current limit
- Input Under Voltage Lockout
- Over-Temperature Protection
- 1.1mA Quiescent Current
- Thermal Enhanced PSOP-8 Package
- RoHS Compliant, 100%Pb & Halogen Free

Applications

- Set-Top-Box
- DVD, LCD Displays
- Networking Device
- Distributed Power System

Functional Block Diagram



Typical Applications

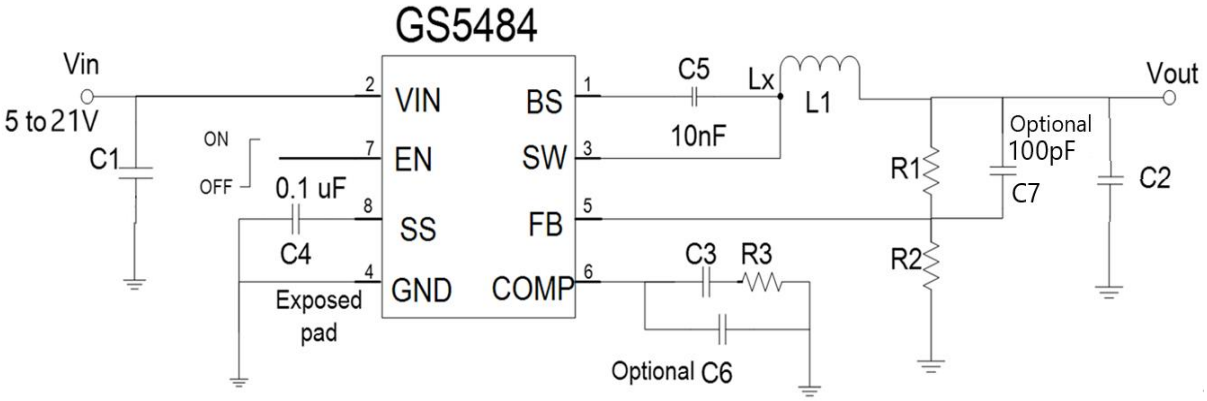
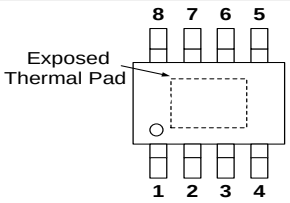


Table 1 recommended Component Selection

V_{OUT}	R1	R2	R3	C3	L1	C2	C1
5.0V	44.2K	10K	7.5K	3.3nF	10 μH	22 x2+0.1 μF	10 x2+0.1 μF
3.3V	26.1K	10K	6.8K	3.3nF	10 μH	22 x2+0.1 μF	10 x2+0.1 μF
2.5V	17K	10K	5.6K	3.3nF	6.8 μH	22 x2+0.1 μF	10 x2+0.1 μF
1.8V	9.4K	10K	4.7K	3.3nF	6.8 μH	22 x2+0.1 μF	10 x2+0.1 μF
1.2V	3.9K	10K	3.9K	3.3nF	4.7 μH	22 x2+0.1 μF	10 x2+0.1 μF
1.0V	1.3K	15K	3.3K	3.3nF	3.3 μH	22 x2+0.1 μF	10 x2+0.1 μF

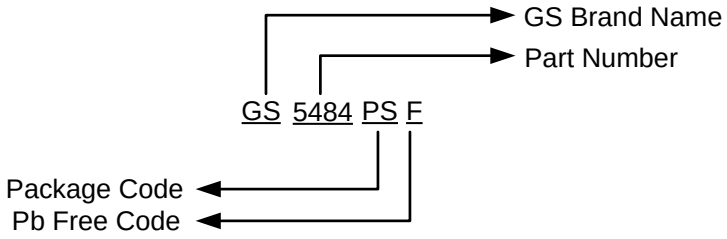
Packages & Pin Assignments

GS5484PSF (PSOP-8)



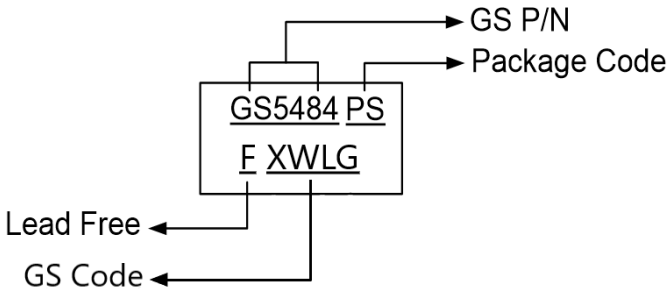
Name	No.	Description
BS	1	High Side Gate Drive Boost Input. A 10nF or greater capacitor must be connected from this pin to SW. It can boost the gate drive to fully turn on the internal high side NMOS.
V_{IN}	2	Power Supply Input Pin. Drive 5V to 21V voltage to this pin to power on this chip. Connecting a 10uF ceramic bypass capacitor between V_{IN} and GND to eliminate noise.
SW	3	Power Switching Output. It is the output pin that internal high side NMOS switching to supply power.
GND	4	Ground Pin. Connecting this pin to exposed pad.
FB	5	Voltage Feedback Input Pin. Connecting FB and V_{OUT} with a resistive voltage divider.
COMP	6	Compensation Pin. This pin is used to compensate the regulation control loop. Connect a series RC network from COMP pin to GND.
EN	7	Enable Input Pin. This pin provides a digital control to turn the converter on or off. Connect to V_{IN} with a 100KΩ resistor for self-startup.
SS	8	Soft-Start Input Pin. This pin controls the soft-start period. Connect a capacitor from SS to GND to set the soft start period.

Ordering Information



Order Number	Package Code	Package	Quantity
GS5484PSF	PS	PSOP-8	4000 PCS/Tape & Reel

Marking Information



Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Max	Units
Input Supply Voltage	V_{IN}	-0.3 to +25	V
SW Voltage	V_{SW}	-1 ~(V_{IN} +0.3)	V
Boost Voltage	V_{BS}	(V_{SW} – 0.3)~(V_{SW} +5)	V
All Other Pins Voltage		-0.3 to +6	V
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-65~150	°C
Lead Temperature (Soldering 10 sec)		260	°C
ESD Rating (Human Body Mode)	HBM	4	KV
ESD Rating (Machine Mode)	MM	300	V

Recommended Operating Conditions (Note 2)

Parameter	Symbol	Max	Units
Input Supply Voltage	V_{IN}	5 to +21	V
Output Voltage	V_{OUT}	0.922~15	V
Ambient Temperature	T_A	-40~85	°C
SOP-8 (Exposed Pad)	θ_{JA}	50	°C/W
SOP-8 (Exposed Pad)	θ_{Jc}	10	°C/W

Note 1: Stresses exceed those ratings may damage the device.
Note 2: If out of its operation conditions, the device is not guaranteed to function.

Electrical Characteristics

(V_{IN}=12V, T_A=25℃, unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Units
V_{IN} Input Supply Voltage		5		21	V
V_{IN} Supply Current	V_{EN}=2.0V		1.1		mA
V_{IN} Shutdown Supply Current	V_{EN}=0V			25	μA
Feedback Voltage	5V≦V_{IN}≦21V	0.904	0.922	0.94	V
High-Side MOSFET $R_{DS(ON)}$			90		mΩ
Low-Side MOSFET $R_{DS(ON)}$			80		mΩ
High-Side MOSFET Leakage Current	V_{EN} = 0V V_{SW} = 0V			10	μA
Current Limit		5			A
COMP to Current sense Transconductance			4.2		A/V
Error Amplifier Transconductance	ΔI_{COMP} = ±10μA		800		μA/V
Error Amplifier Voltage Gain			400		V/V
Oscillation frequency			340		KHz
Short Circuit Oscillation Frequency	V_{FB} = 0V		100		KHz
Maximum Duty Cycle	V_{FB} = 0.8V		90		%
Minimum On Time			200		ns
Input UVLO Threshold	V_{IN} Rising		4.75		V
Under Voltage Lockout Threshold Hysteresis			400		mV
Soft-Start Period	C_{SS} = 0.1uF		15		ms
EN Input Threshold Voltage	V_{EN} Rising		1.5		V
EN Input low current			0.1		μA
Thermal Shutdown Threshold			160		℃
Thermal Shutdown hysteresis			20		℃

Typical Operating Characteristics

V_{IN}=12V, V_{OUT}=5.0V, C1 = 10uF , C2 = 22uF, L1 = 15uH, T_A = +25℃, unless otherwise noted.

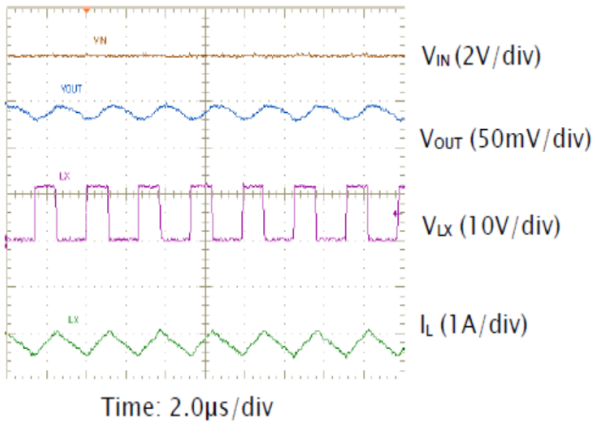


Figure1. Steady State Operation

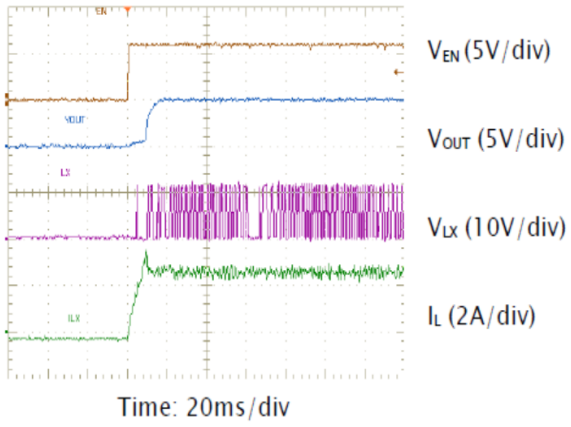


Figure2. Start-Up Through Enable

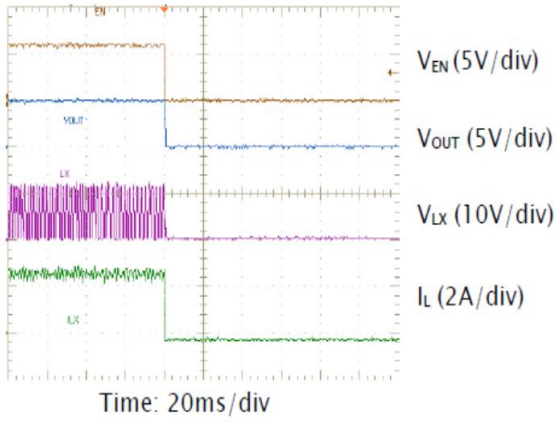


Figure3. Shutdown Through Enable

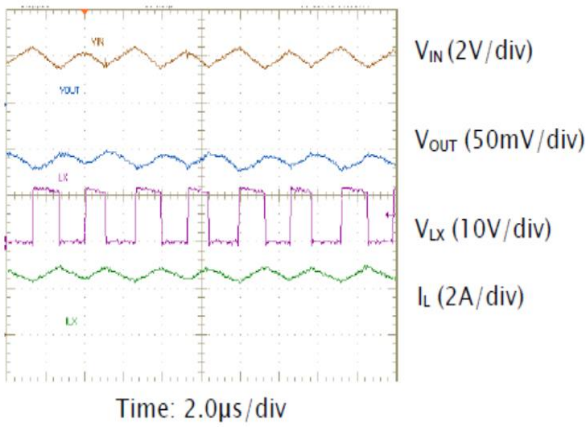


Figure4. Heavy Load (3A) Operation

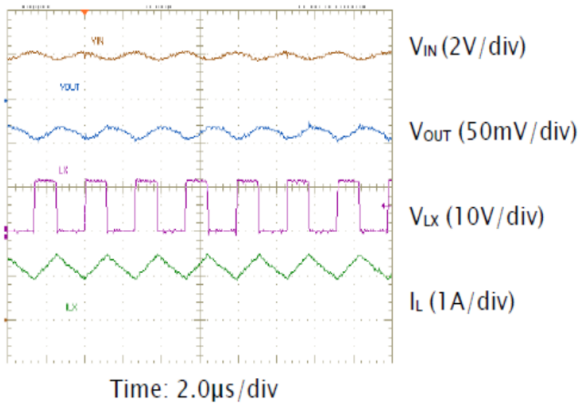


Figure5. Medium Load (1.5A) Operation

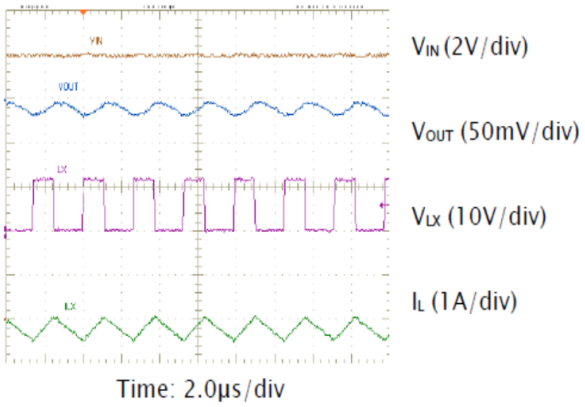


Figure6. Light Load (no load) Operation

Typical Operating Characteristics(cont.)

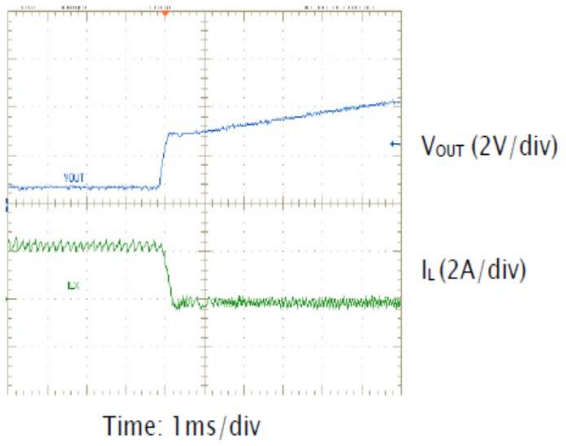


Figure7. Heavy Load (3A) Short Circuit Recovery

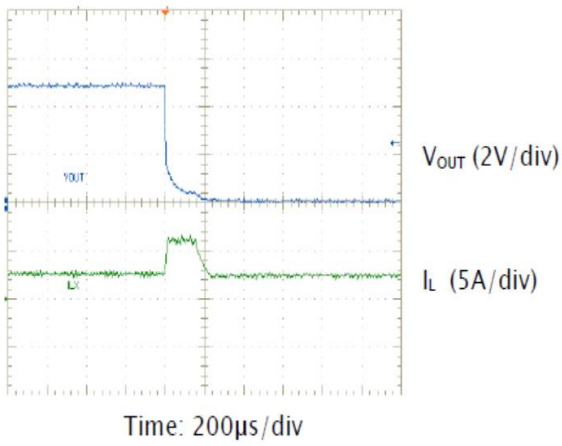


Figure8. Heavy Load (3A) Short Circuit Protection

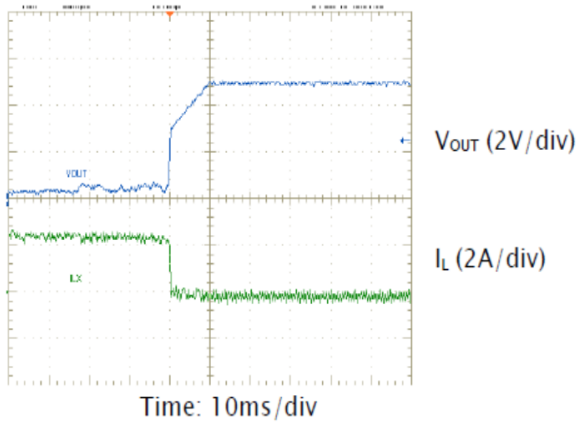


Figure9. Light Load (no load) Short Circuit Recovery

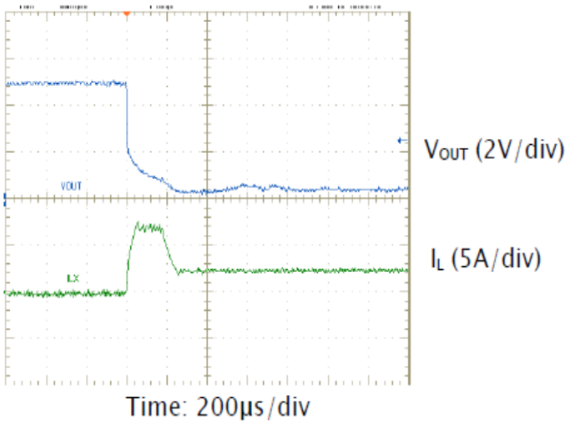


Figure10. Light Load (no load) Short Circuit Protection

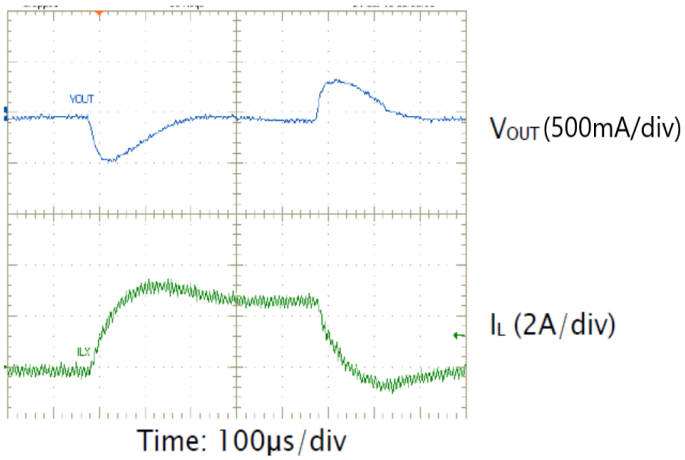


Figure11. Load Transient

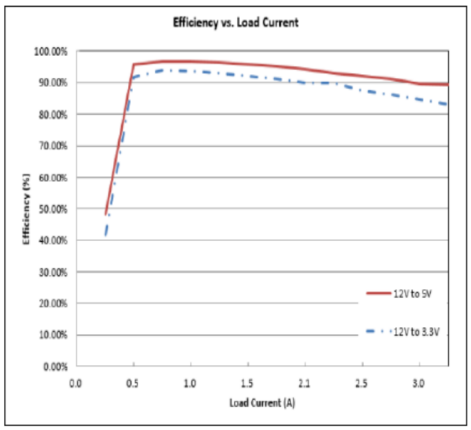


Figure12. Efficiency

Function Description

The GS5484 is a constant frequency current mode step-down synchronous DC/DC converter. It regulates input voltage from 5V to 21V, down to an output voltage as low as 0.922V and can provide 3A of continuous load current.

Control Loop

During normal operation, the output voltage is sensed at FB pin through a resistive voltage divider and amplified through the error amplifier. The voltage of error amplifier output pin – COMP is compared to the switch current to controls the RS latch. At each cycle, the high side NMOS would be turned on when the oscillator sets the RS latch and would be turned off when current comparator resets the RS latch. When the load current increases, the FB pin voltage drops below 0.922V, it causes the COMP voltage increase until average inductor current arrive at new load current.

Enable

The GS5484 EN pin provides digital control to turn on/turn off the regulator. When the voltage of EN exceeds the threshold voltage, the regulator starts the soft start function. If the EN pin voltage is below than the threshold voltage, only the bandgap voltage is alive. If the EN pin voltage is below than the shutdown threshold voltage, the regulator will be disable and into the shutdown mode.

Maximum Load Current

The maximum load current decreases at lower input voltage because of large IR drop on the high side switch and low side switch. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%.

Input Under Voltage Lockout

When the GS5484 power on, the internal circuits are held inactive until V_{IN} exceeds the input UVLO threshold voltage. And the regulator will be disabled when V_{IN} below the input UVLO threshold voltage.

Short Circuit Protection

The GS5484 provides short circuit protection function to prevent the device damage from short condition. When the output short to ground, the oscillator frequency is reduced to prevent the inductor current increasing beyond the current limit. In the meantime, the current limit is also reduced to lower the short current. Once the short condition is removed, the frequency and current limit will return to normal.

Over Temperature Protection

The GS5484 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown.

Compensation

The stability of the feedback circuit is controlled through COMP pin. The compensation value of the application circuit is optimized for particular requirements. If different conversions are requires, some of the components may need to be changes to ensure stability.

Application Information

Output Voltage Setting

The output voltage V_{OUT} is set using a resistive divider from the output to FB. The FB pin regulated voltage is 0.922V. Thus the output voltage is:

$$V_{OUT} = 0.922 \times \left(1 + \frac{R1}{R2}\right) V$$

R2 recommended value is 10kΩ, so R1 is determined by:

$$R1 = 10.83 \times (V_{OUT} - 0.922) k\Omega$$

Table 1 lists recommended values of R1 and R2 for most used output voltage.

Table 2 Recommended Resistance Values

V_{OUT}	R1	R2
5V	44.2kΩ	10kΩ
3.3V	26.1kΩ	10kΩ
2.5V	17.0kΩ	10kΩ
1.8V	9.4kΩ	10kΩ

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

Input Capacitor Selection

The use of the input capacitor is controlling the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 times to 1.5 times greater than the maximum input voltage.
The input capacitor ripple current RMS value is
calculated as:

$$I_{IN(RMS)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

Where D is the duty cycle of the power MOSFET.
A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a 0.1uF ceramic capacitor should be placed as close to the IC as possible.

Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. Low ESR capacitors are preferred. Ceramic, tantalum or low ESR electrolytic capacitors can be used, depends on the output ripple requirement. Add a 100uF or 470uF Low ESR electrolytic capacitor when operated in high input voltage range (V_{IN} > 20V). It can improve the device's stability. The output ripple voltage ΔV_{OUT} is described as:

$$\Delta I = \frac{V_{OUT}}{Fosc \times L} \times \left(1 - \frac{Vout}{Vin}\right)$$

$$\Delta V_{OUT} = \Delta I \times \left(R_{ESR} + \frac{1}{8 \times Fosc \times Cout}\right)$$

Where Δ I is the peak-to-peak inductor ripple current, FOSC is the switching frequency, L is the inductance value, V_{IN} is the input voltage, V_{OUT} is the output voltage, RESR is the equivalent series resistance value of the output capacitor, and the C_{OUT} is the output capacitor. When using the ceramic capacitors, the RESR can be ignored and the output ripple voltage ΔV_{OUT} is shown as:

$$\Delta V_{OUT} = \frac{\Delta I}{8 \times Fosc \times C_{OUT}}$$

When using tantalum or electrolytic capacitors, typically 90% of the output voltage ripple is contributed by the ESR of output capacitors. the output ripple voltage ΔV_{OUT} can be estimated as:

$$\Delta V_{OUT} = \Delta I \times R_{ESR}$$

Output Inductor Selection

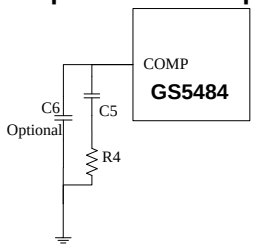
The output inductor is used for store energy and filter output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode. That will lower ripple current and results in lower output ripple voltage. A good rule for determining the inductance is set the peak-to-peak inductor ripple current Δ I almost equal to 30% of the maximum load current. Then the minimum inductance can be calculated with the following equation:

$$\Delta I = 0.3 \times I_{OUT}(max)$$

$$L \geq (V_{IN} - V_{OUT}) \times \left(\frac{V_{OUT}}{Fosc \times \Delta I \times V_{IN}}\right)$$

Where V_{IN} is the maximum input voltage.

Compensation Components Selection



Selecting the appropriate compensation value by following procedure:
1. Calculate the R4 value with the following equation:

$$R4 < \frac{2\pi \times C_{OUT} \times 0.1 \times Fosc \times V_{OUT}}{G_{EA} \times Gcs \times V_{REF}}$$

where G_{EA} is the error amplifier voltage gain, and G_{CS} is the current sense gain.

2. Calculate the C5 value with the following equation:

$$C5 > \frac{4}{2\pi \times R4 \times 0.1 \times Fosc}$$

3. If the COUT ESR zero is less than half of the switching frequency, use C6 to cancel the ESR zero:

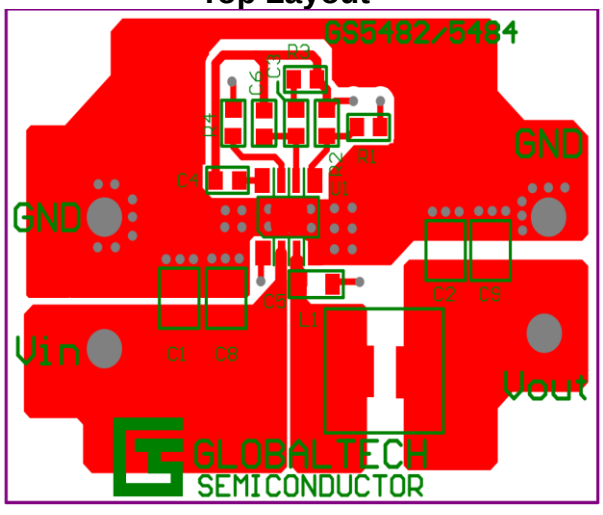
$$C6 = \frac{C_{OUT} \times R_{ESR}}{R4}$$

PCB Layout Recommendation

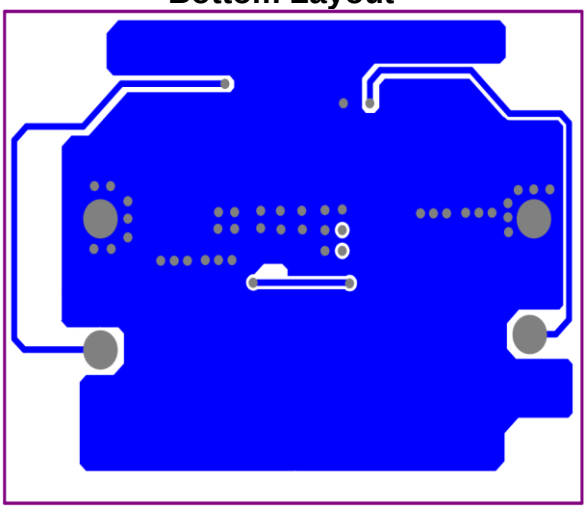
The device's performance and stability is dramatically affected by PCB layout. It is recommended to follow these general guidelines show bellow:

1. Place the input capacitors, output capacitors as close to the device as possible. Trace to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{IN} bypass capacitors close to the V_{IN} pin.
3. Place feedback resistors close to the FB pin.
4. Place compensation components close to the COMP pin.
5. Keep the sensitive signal (FB, COMP) away from the switching signal (SW).
6. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connects to the exposed pad should be maximized to improve thermal performance.
7. Multi-layer PCB design is recommended.

Top Layout

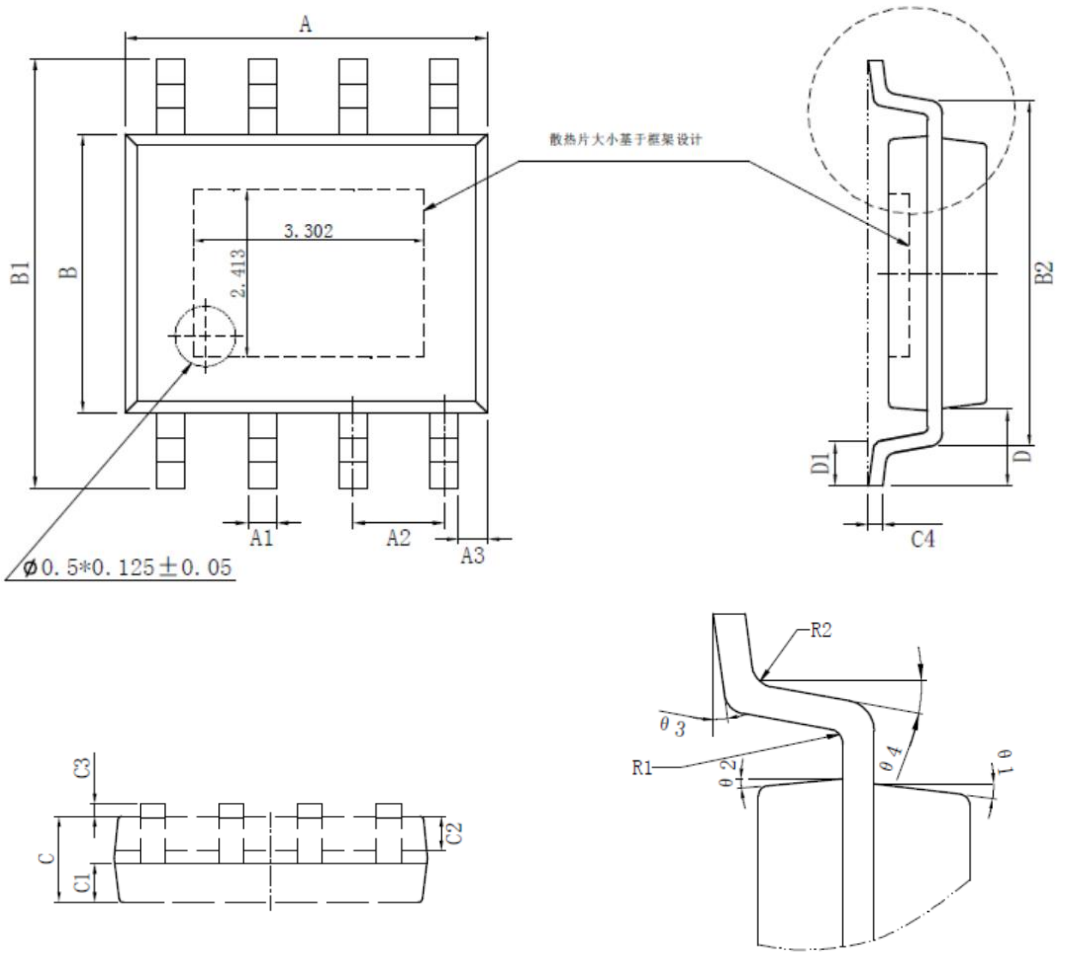


Bottom Layout



Package Dimension

PSOP-8



Dimensions					
SYMBOL	Millimeters		SYMBOL	Millimeters	
	MIN	MAX		MIN	MAX
A	4.80	5.00	C3	0.00	0.09
A1	0.356	0.456	C4	0.203	0.233
A2	1.27 TYP		D	1.05 TYP	
A3	0.345 TYP		D1	0.40	0.80
B	3.80	4.00	R1	0.20 TYP	
B1	5.80	6.20	R2	0.20 TYP	
B2	5.00 TYP		θ1	17° TYP	
C	1.30	1.60	θ2	13° TYP	
C1	0.55	0.65	θ3	0°~8°	
C2	0.55	0.65	θ4	4°~12°	

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