

GS534063

DC-To-DC Converter Control Circuits

Product Description

The GS534063 Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters.

These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch.

This series was specifically designed to be incorporated in Step-Down and step-Up and Voltage-Inverting applications with a minimum number of external components.

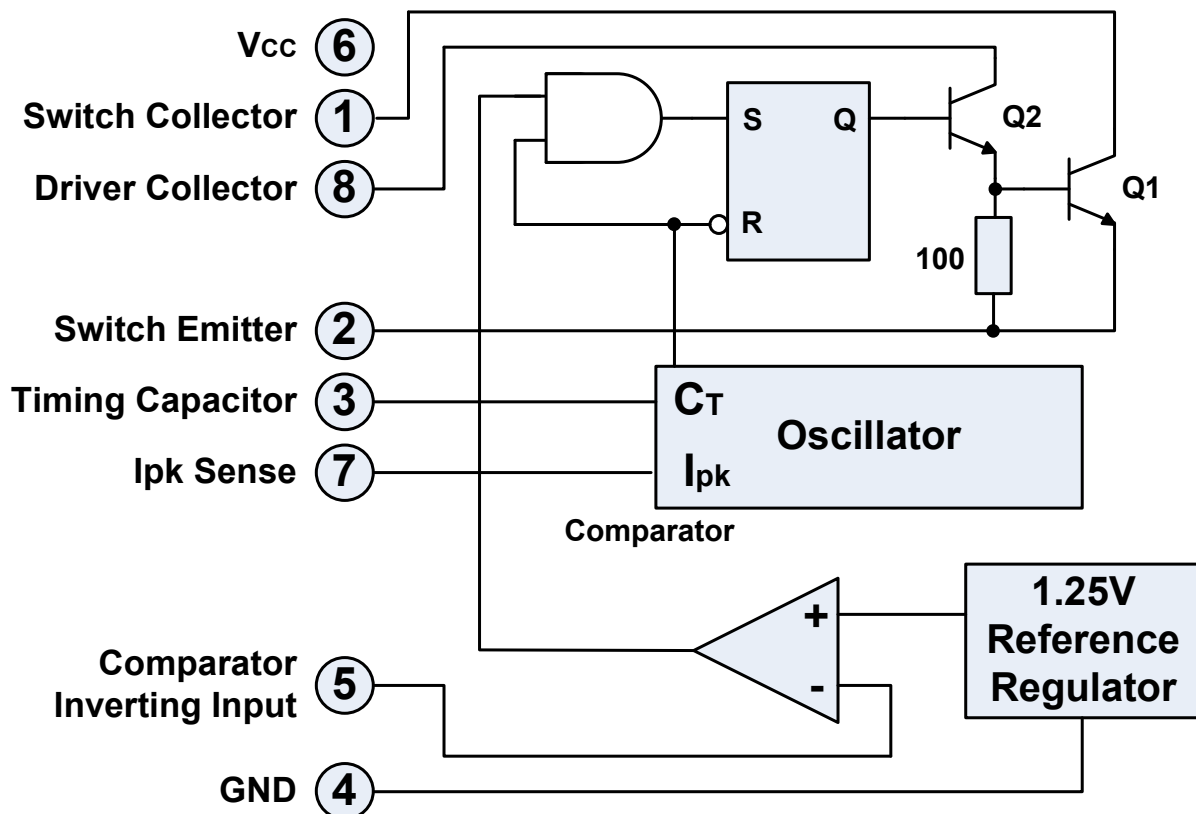
Features

- Operation from 3.0V to 40V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5A
- Output Voltage Adjustable
- Frequency Operation to 100kHz
- Precision 2% Reference

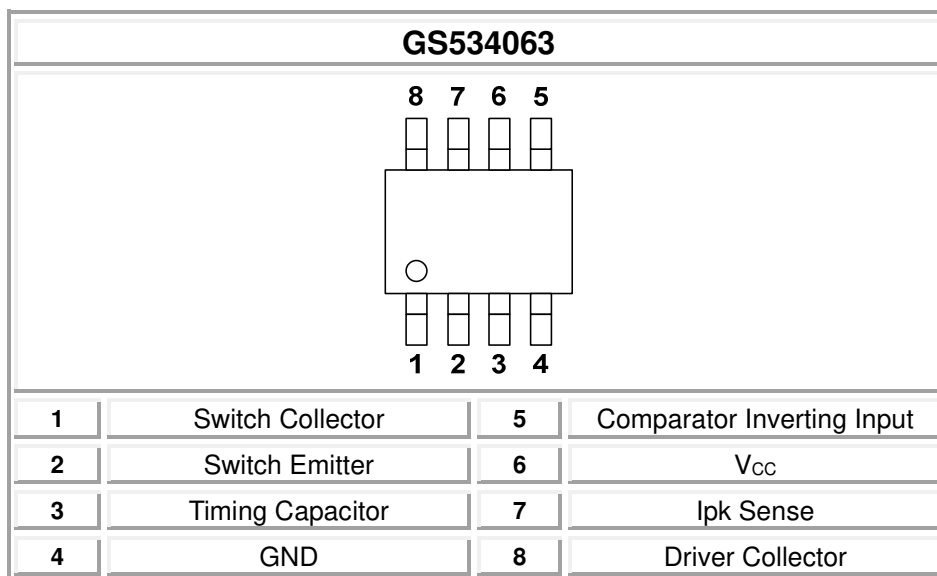
Applications

- Battery Powered Applications
- Laptop/Notebook Computers
- Power Inverter (+ to -) or (- to +)
- Medical Instruments
- Interface Power Supplies
- Portable Instruments
- Cellular Phones/Radio

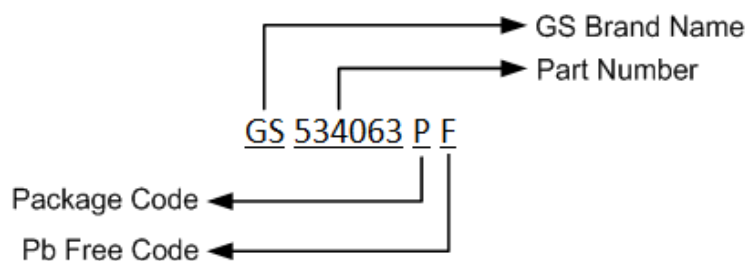
Block Diagram



Packages & Pin Assignments



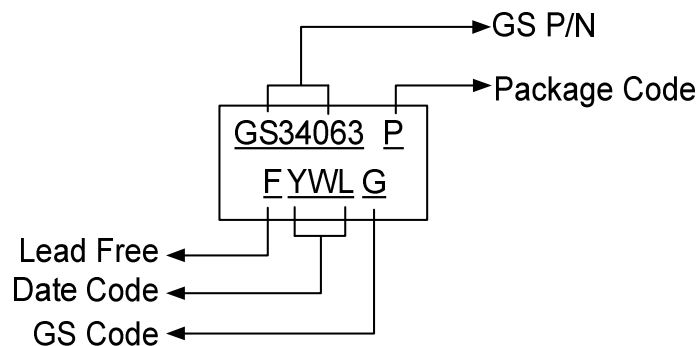
Ordering Information



Device	Package
GS534063PF	DIP-8
GS534063SF	SOP-8

For additional available fixed voltages, please contact factory.

Marking Information



Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit
V _{CC}	Power Supply Voltage	40		V
V _{IR}	Comparator Input Voltage Range	-0.3 to +40		V
V _{C(switch)}	Switch Collector Voltage	40		V
V _{E(switch)}	Switch Emitter Voltage (V _{PIN1} =40V)	40		V
V _{CE(switch)}	Switch Collector to Emitter Voltage	40		V
V _{C(driver)}	Driver Collector Voltage	40		V
I _{C(driver)}	Driver Collector Current (Note 1)	100		mA
I _{sw}	Switch Current	1.5		A
P _D	Power Dissipation T _A =25°C	SOP-8	0.625	W
		DIP-8	1.25	
θ _{Jc}	Thermal Resistance(Junction to Case) T _A =25°C	SOP-8	20	°C/W
		DIP-8	45	
θ _{JA}	Thermal Resistance(Junction to Ambient) T _A =25°C	SOP-8	150	°C/W
		DIP-8	100	
T _J	Operating Junction Temperature	+150		°C
T _A	Operating Ambient Temperature Range	-20 to +70		°C
T _{STG}	Storage Temperature Range	-65 to +150		°C

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Oscillator						
F_{OSC}	Frequency	$V_{pin5}=0V$, $C_T=1.0nF$, $T_A=25^{\circ}C$	24	33	42	kHz
I_{CHG}	Charge Current	$V_{CC}=5.0V$ to $40V$, $T_A=25^{\circ}C$	24	35	42	μA
I_{DISCHG}	Discharge Current	$V_{CC}=5.0V$ to $40V$, $T_A=25^{\circ}C$	140	220	260	μA
I_{DISCHG} / I_{CHG}	Discharge to Charge Current Ratio	Pin 7 to V_{CC} , $T_A=25^{\circ}C$	5.2	6.5	7.5	--
$V_{IPK(SENCE)}$	Current Limit sense Voltage	$I_{CHG}=I_{DISCHG}$, $T_A=25^{\circ}C$	250	300	350	mV
Output Switch (NOTE 2)						
$V_{CE(sat)}$	Saturation Voltage, Darlington Connection	$I_{SW}=1.0A$, Pins 1, 8 connected	--	1.0	1.3	V
$V_{CE(sat)}$	Saturation Voltage, Darlington Connection	$I_{SW}=1.0A$, $R_{PIN8}=82\Omega$ to V_{CC} , Forced $\beta \cong 20$	--	0.45	0.7	V
H_{FE}	DC Current Gain	$I_{SW}=1.0A$, $V_{CE}=5.0V$, $T_A=25^{\circ}C$	50	75	--	--
$I_{C(off)}$	Collector Off-state Current	$V_{CE}=40V$	--	40	100	μA
Comparator						
V_{TH}	Threshold Voltage	$T_A=25^{\circ}C$ ($T_A=T_{LOW}$ to T_{HIGH})	1.225 1.21	1.25 --	1.275 1.29	V
$REG_{(LINE)}$	Threshold Voltage Line Regulation	$V_{CC}=3.0V$ to $40V$	--	1.4	5.0	mV
I_{IB}	Input Bias Current	$V_{in}=0V$	--	-20	-400	nA
Total Device						
I_{CC}	Supply Current	$V_{CC}=5.0V$ to $40V$, $C_T=1.0nF$, Pin 7= V_{CC} , $V_{PIN5}>V_{TH}$, Pin 2=GND, remaining pins open	--	--	4.0	mA

NOTE1:Maximum package power dissipation limits must be observed.

NOTE2:Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

Typical Performance Characteristics

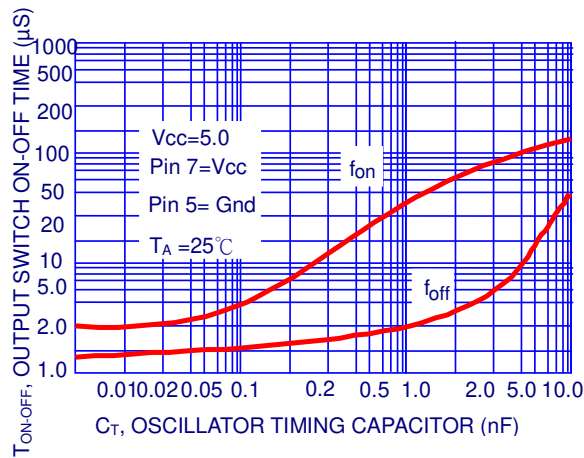


Figure 1.
Output Switch On-Off Time Versus Oscillator Timing Capacitor

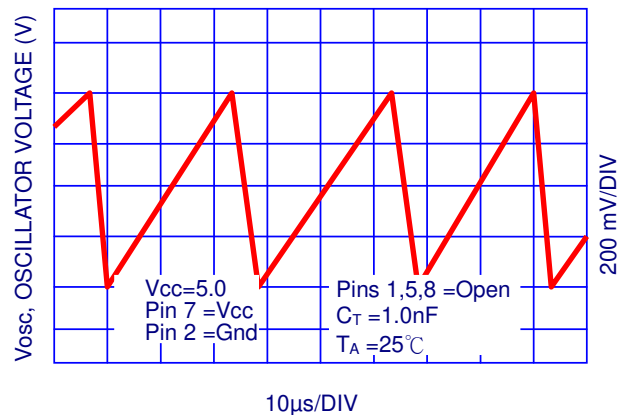


Figure 2
Timing Capacitor Waveform.

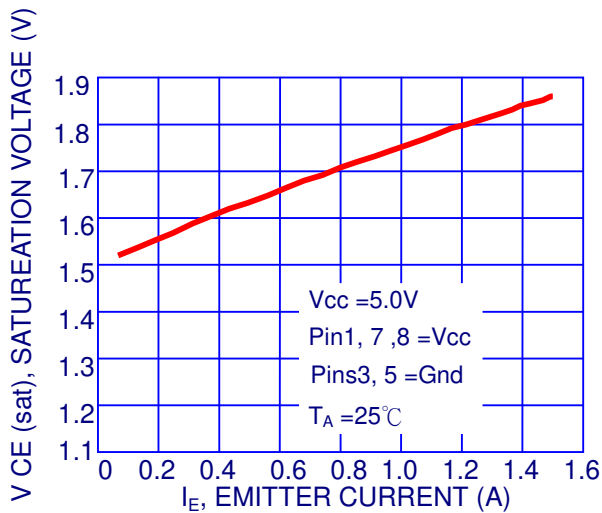


Figure 3.
Emitter Follower Configuration Output Saturation Voltage versus Emitter Current

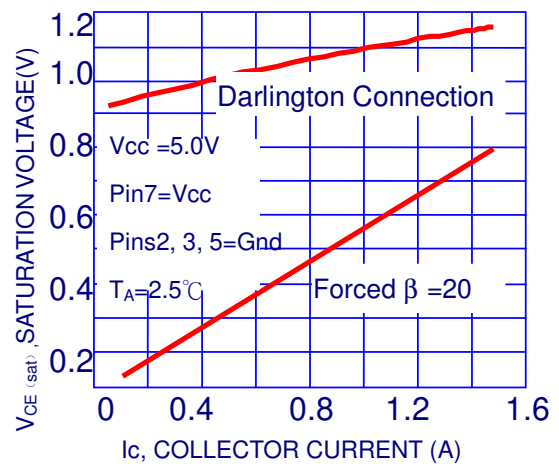


Figure 4.
Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current

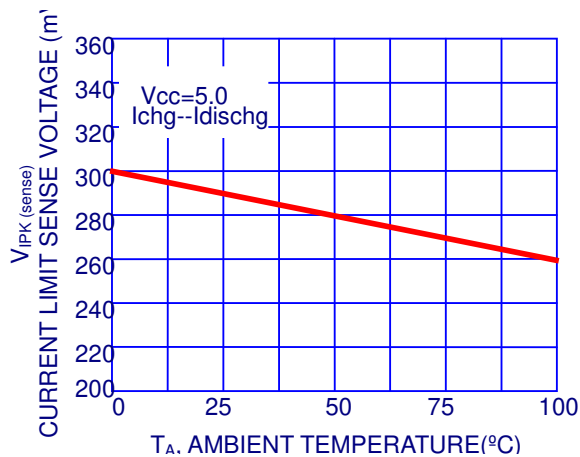


Figure 5.
Current Limit Sense Voltage versus Temperature

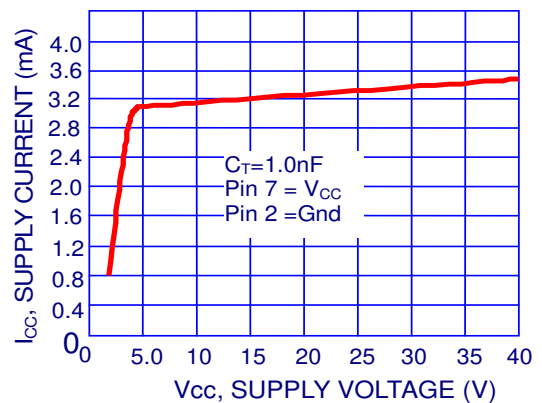
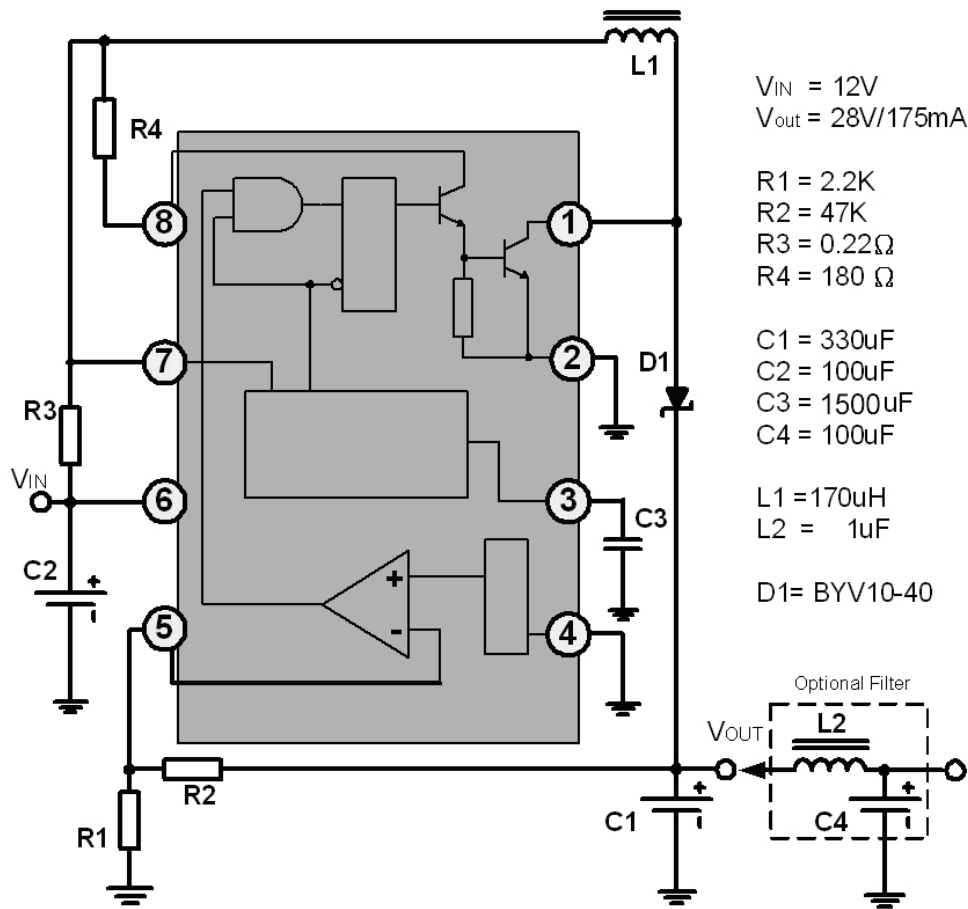
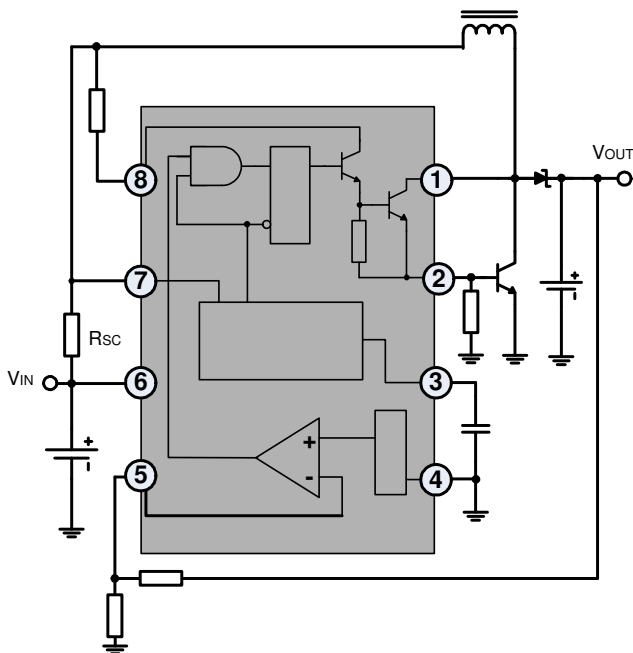


Figure 6.
Standby Supply Current versus supply Voltage

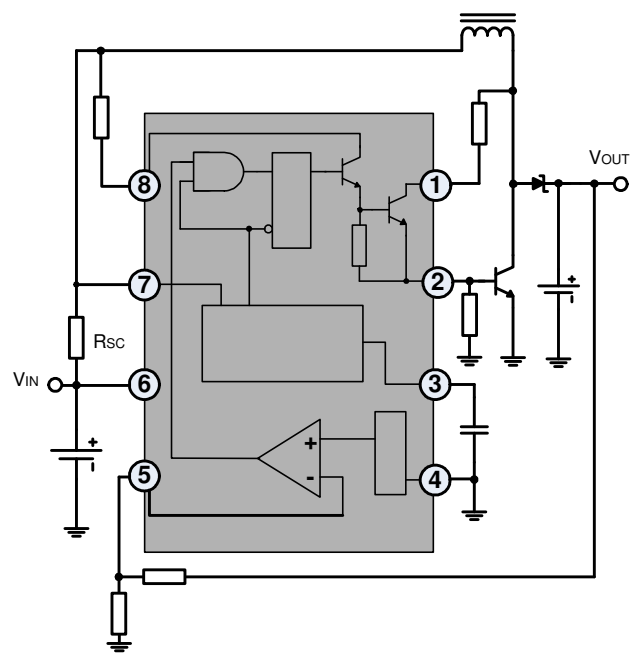
Typical Applications Circuit



Step-Up Converter

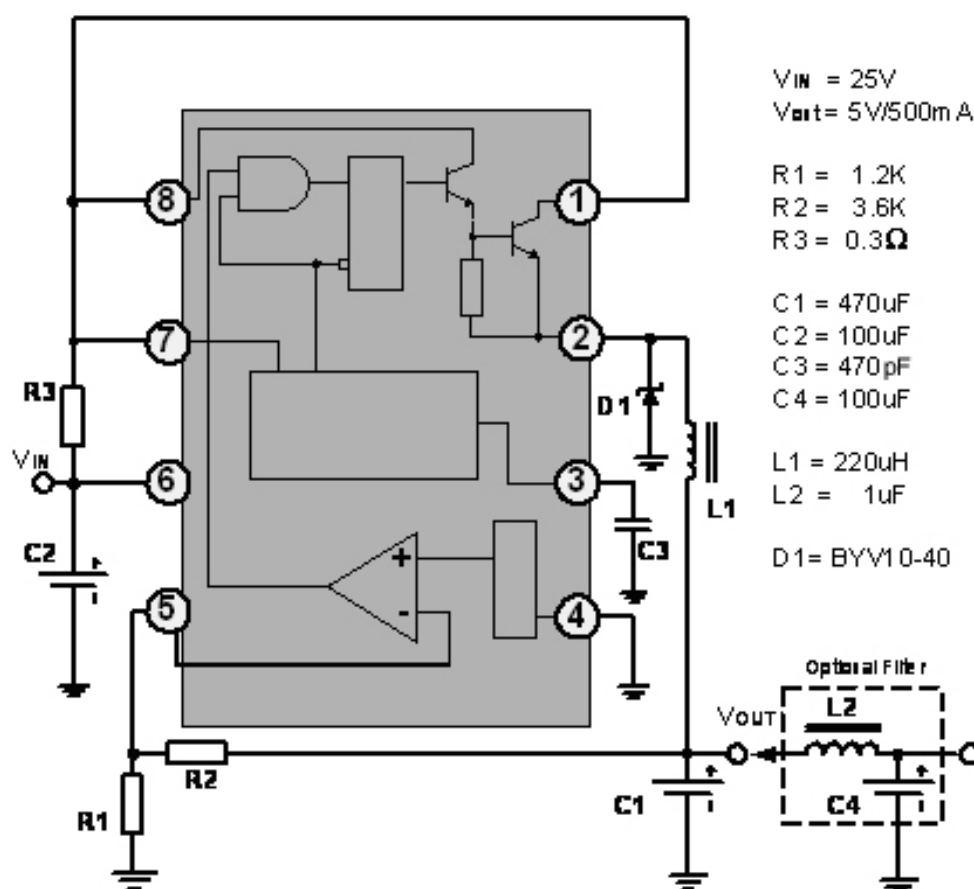


Step-Up With
External NPN Switch

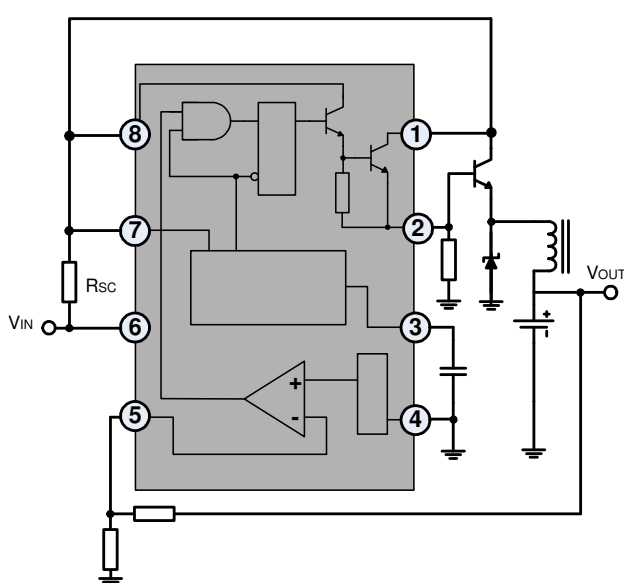


Step-Up With
External NPN Saturated Switch (See Note 5)

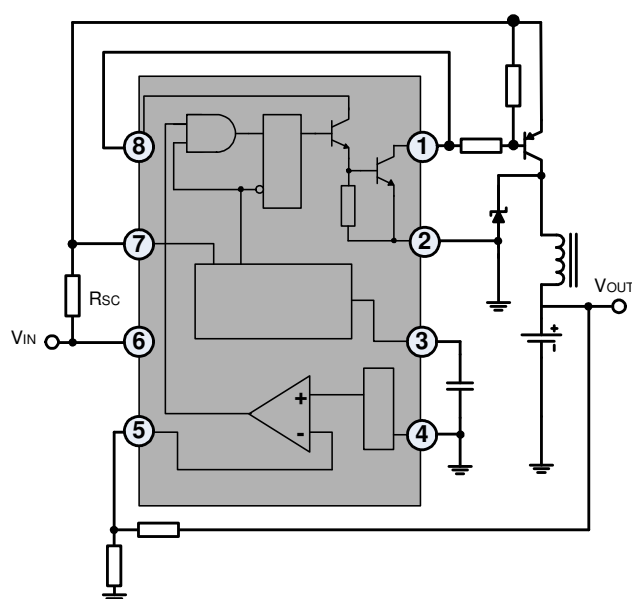
Typical Applications Circuit (Continued)



Step-Down Converter

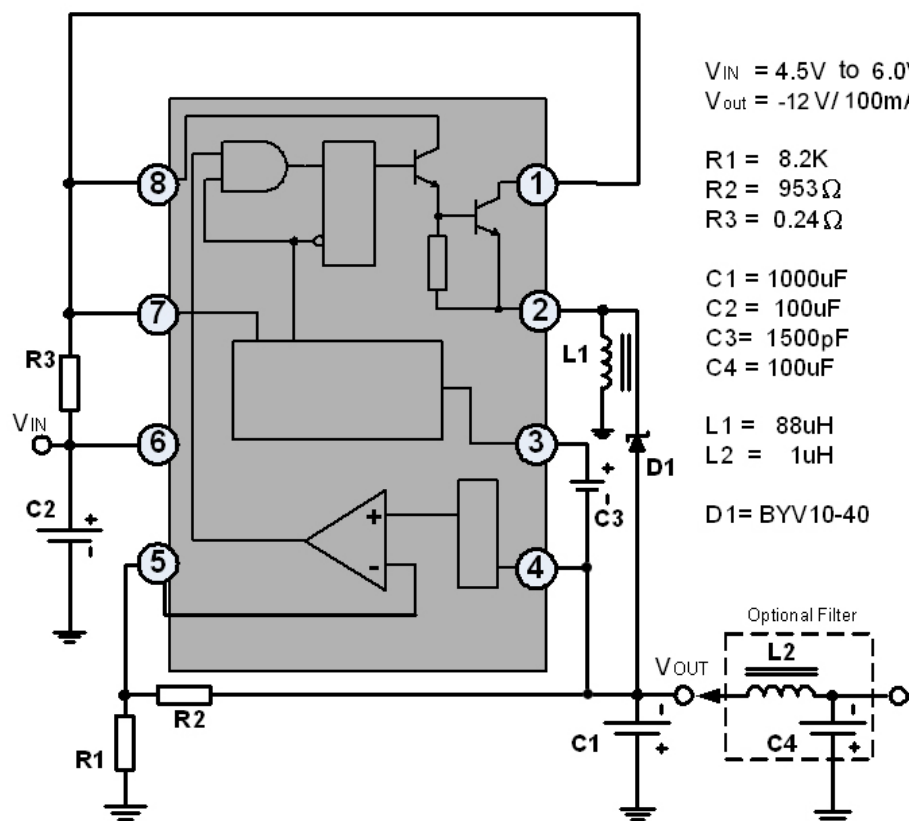


Step-Down With External NPN Switch

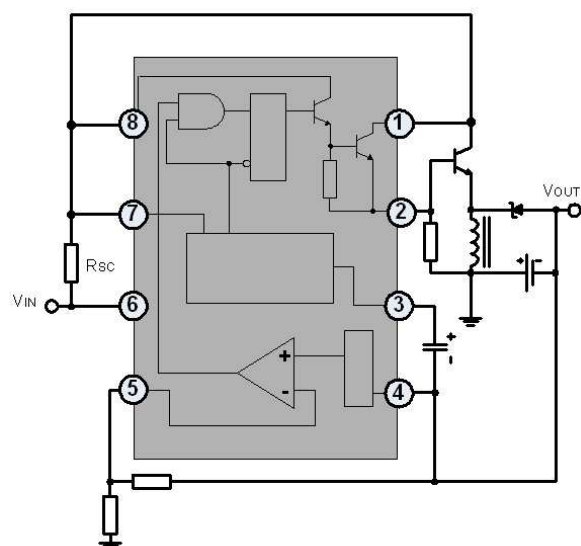


Step-Down With External PNP Saturated Switch

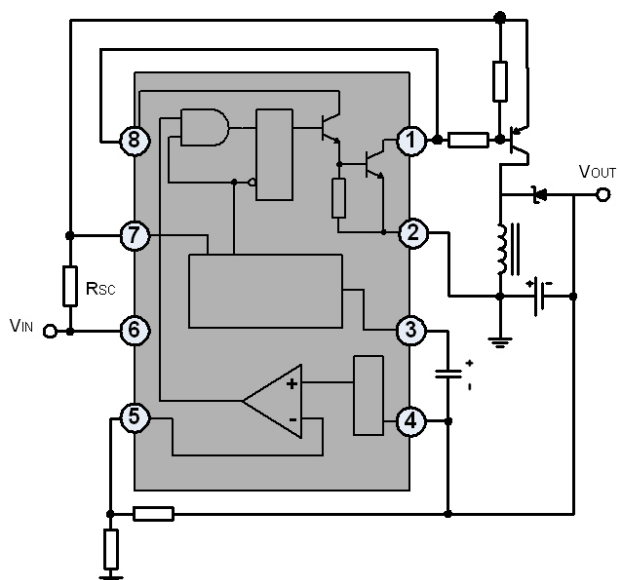
Typical Applications Circuit (Continued)



Voltage Inverting Converter

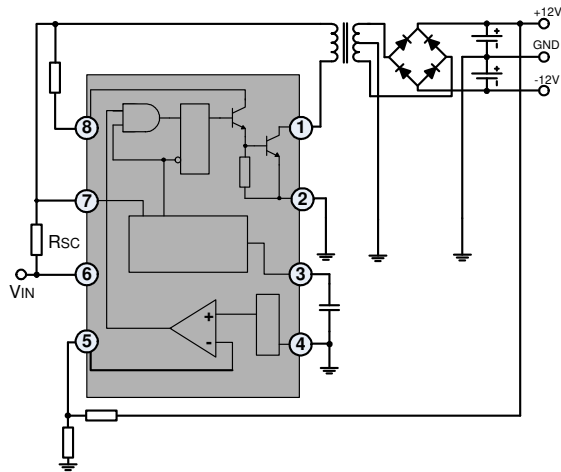


Voltage Inverting With
External NPN Switch

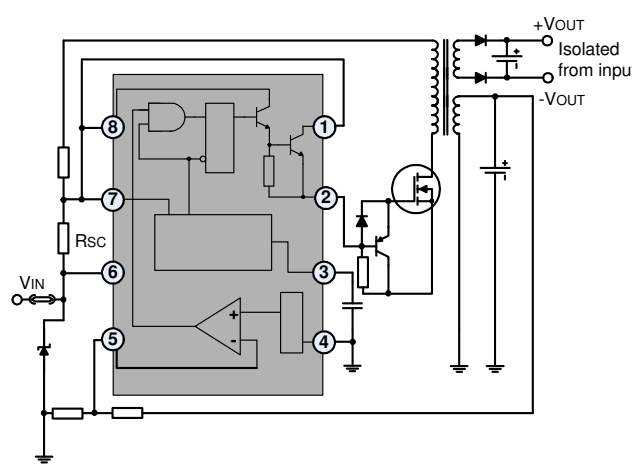


Voltage Inverting With
External NPN Saturated Switch

Typical Applications Circuit (Continued)



Dual Output Voltage



**Higher Output Power ,
Higher Input Voltage**

Design Formula Table

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{ON} / t_{OFF}	$\frac{V_{OUT} + V_F - V_{IN(MIN)}}{V_{IN(MIN)} - V_{SAT}}$	$\frac{V_{OUT} + V_F}{V_{IN(MIN)} - V_{SAT} - V_{OUT}}$	$\frac{ V_{OUT} + V_F}{V_{IN} - V_{SAT}}$
$(t_{ON} + t_{OFF})_{MAX}$	$\frac{1}{f_{MIN}}$	$\frac{1}{f_{MIN}}$	$\frac{1}{f_{MIN}}$
C_T	$4.0 \times 10^{-5} t_{ON}$	$4.0 \times 10^{-5} t_{ON}$	$4.0 \times 10^{-5} t_{ON}$
$I_{PK(SWITCH)}$	$2 I_{OUT(MAX)} \left(\frac{t_{ON}}{t_{OFF}} + 1 \right)$	$2 I_{OUT(MAX)}$	$2 I_{OUT(MAX)} \left(\frac{t_{ON}}{t_{OFF}} + 1 \right)$
R_{SC}	$0.3 / I_{PK(SWITCH)}$	$0.3 / I_{PK(SWITCH)}$	$0.3 / I_{PK(SWITCH)}$
$L_{(MIN)}$	$\frac{V_{IN(MIN)} - V_{SAT}}{I_{PK(SWITCH)}} t_{ON(MAX)}$	$\frac{V_{IN(MIN)} - V_{SAT} - V_{OUT}}{I_{PK(SWITCH)}} t_{ON(MAX)}$	$\frac{V_{IN(MIN)} - V_{SAT}}{I_{PK(SWITCH)}} t_{ON(MAX)}$
C_O	$9 \frac{I_{OUT} t_{ON}}{V_{RIPPLE(PP)}}$	$\frac{I_{PK(SWITCH)} (t_{ON} + t_{OFF})}{8 V_{RIPPLE(PP)}}$	$9 \frac{I_{OUT} t_{ON}}{V_{RIPPLE(PP)}}$

Terms And Defintions

V_{SAT} : Saturation voltage of the output switch.

V_F : Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{IN} : Nominal input voltage

V_{OUT} : Desired output voltage, $|V_{OUT}| = 1.25(1 + R_2/R_1)$

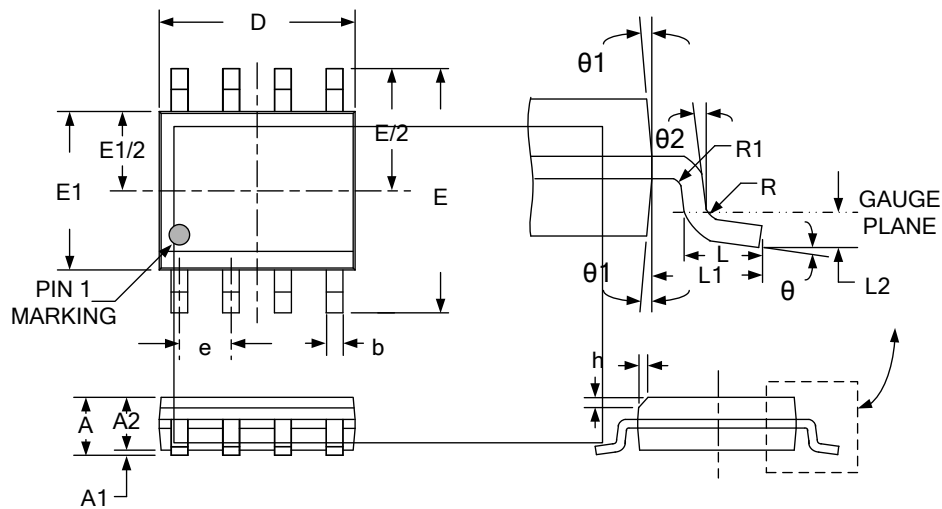
I_{OUT} : Desired output current.

f_{MIN} : Minimum desired output switching frequency at the selected values of V_{in} and I_o .

$V_{RIPPLE(PP)}$: Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to low value since it will directly affect the line and load regulation.

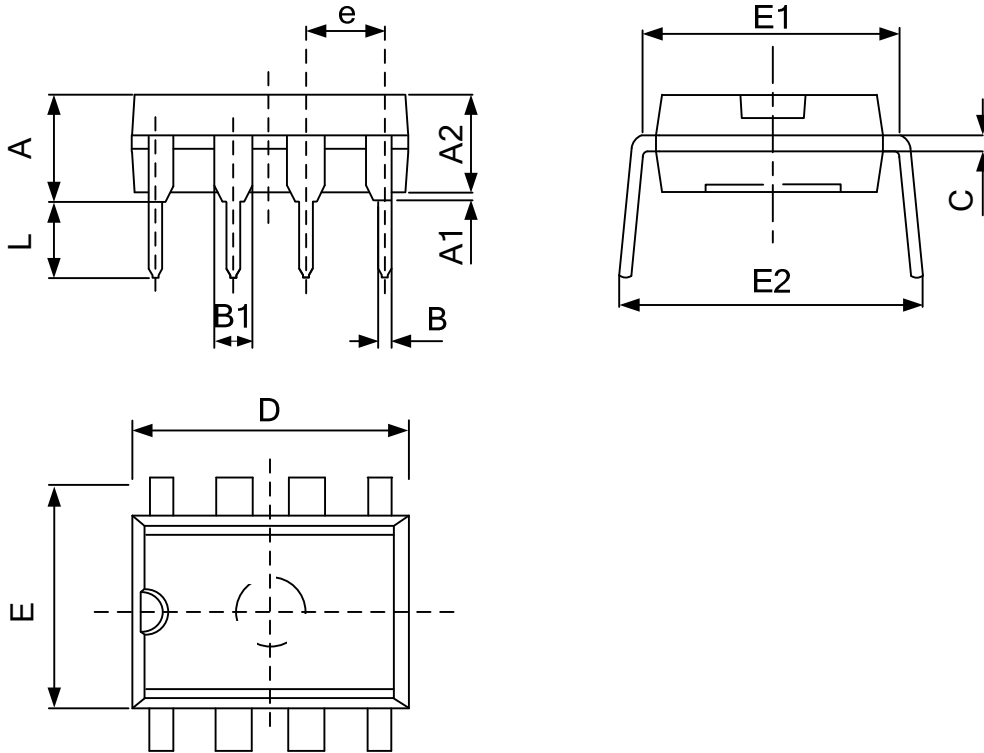
Package Dimension

SOP-8 PLASTIC PACKAGE



Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	1.35	1.75	.053	.069
A1	0.10	0.25	.004	.010
A2	1.25	1.65	.049	.065
b	0.31	0.51	.012	.020
c	0.17	0.25	.007	.010
D	4.90 (TYP)		.193 (TYP)	
E	6.00 (TYP)		.236 (TYP)	
E1	3.90 (TYP)		.154 (TYP)	
e	1.27 (TYP)		.050 (TYP)	
L	0.40	1.27	.016	.050
L1	1.04 (TYP)		.041 (TYP)	
L2	0.25 (TYP)		.010 (TYP)	
R	0.07	-	.003	-
R1	0.07	-	.003	-
h	0.25	0.50	.010	.020
θ	0°	8°	0°	8°
θ_1	5°	15°	5°	15°
θ_2	0°	-	0°	-

DIP-8 PLASTIC PACKAGE



Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	3.710	4.310	.146	.170
A1	0.510	-	.020	-
A2	3.200	3.600	.126	.142
B	0.380	0.570	.015	.022
B1	1.524(BSC)		0.060 (BSC)	
C	0.204	0.360	.008	.014
D	9.000	9.400	.354	.370
E	6.200	6.600	.244	.260
E1	7.320	7.920	.288	.312
e	2.540(BSC)		.100 (BSC)	
L	3.000	3.600	.118	.142
E2	8.400	9.000	.331	.354

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