GS5484 Application Note

Typical Applications Circuit

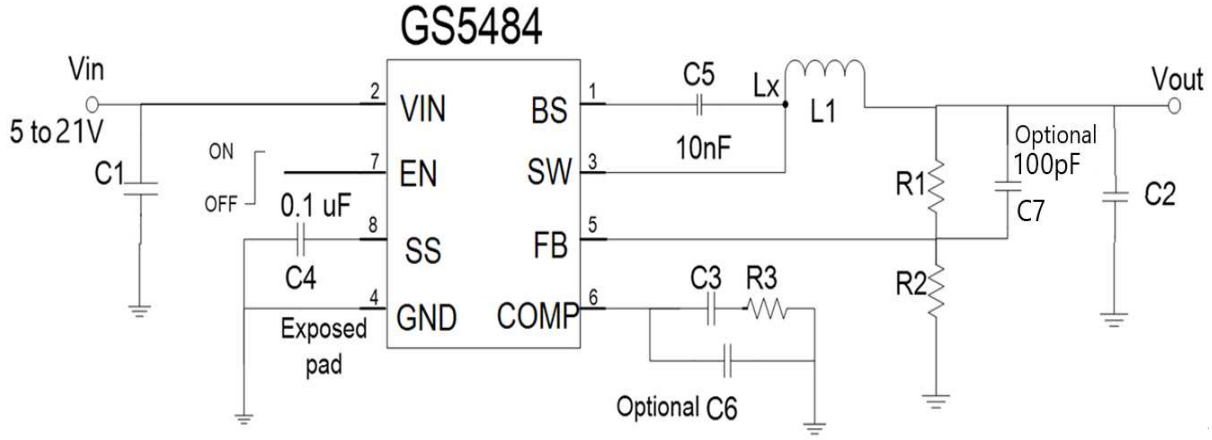

Table 1 recommended Component Selection

V_{OUT}	R1	R2	R3	C3	L1	C2	C1
5.0V	44.2K	10K	7.5K	3.3nF	10 μH	22 x2+0.1 μF	10 x2+0.1 μF
3.3V	26.1K	10K	6.8K	3.3nF	10 μH	22 x2+0.1 μF	10 x2+0.1 μF
2.5V	17K	10K	5.6K	3.3nF	6.8 μH	22 x2+0.1 μF	10 x2+0.1 μF
1.8V	9.4K	10K	4.7K	3.3nF	6.8 μH	22 x2+0.1 μF	10 x2+0.1 μF
1.2V	3.9K	10K	3.9K	3.3nF	4.7 μH	22 x2+0.1 μF	10 x2+0.1 μF
1.0V	1.3K	15K	3.3K	3.3nF	3.3 μH	22 x2+0.1 μF	10 x2+0.1 μF

Output Voltage Setting

The output voltage V_{OUT} is set using a resistive divider from the output to FB. The FB pin regulated voltage is 0.922V.

Thus the output voltage is:

$$V_{OUT} = 0.922 \times \left(1 + \frac{R1}{R2}\right) V$$

R2 recommended value is 10kΩ, so R1 is determined by:

$$R1 = 10.83 \times (V_{OUT} - 0.922) k\Omega$$

Table 1 lists recommended values of R1 and R2 for most used output voltage.

Recommended Resistance Values

V_{OUT}	R1	R2
5V	44.2kΩ	10kΩ
3.3V	26.1kΩ	10kΩ
2.5V	17.0kΩ	10kΩ
1.8V	9.40kΩ	10kΩ

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

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Input Capacitor Selection

The use of the input capacitor is controlling the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 times to 1.5 times greater than the maximum input voltage.
The input capacitor ripple current RMS value is
calculated as:

$$I_{IN(RMS)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

Where D is the duty cycle of the power MOSFET.
A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a 0.1uF ceramic capacitor should be placed as close to the IC as possible.

Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. Low ESR capacitors are preferred. Ceramic, tantalum or low ESR electrolytic capacitors can be used, depends on the output ripple requirement. Add a 100uF or 470uF Low ESR electrolytic capacitor when operated in high input voltage range (V_{IN} > 20V). It can improve the device's stability. The output ripple voltage Δ V_{OUT} is described as:

$$\Delta I = \frac{V_{OUT}}{Fosc \times L} \times \left(1 - \frac{Vout}{Vin}\right)$$

$$\Delta V_{OUT} = \Delta I \times \left(R_{ESR} + \frac{1}{8 \times Fosc \times Cout}\right)$$

Where Δ I is the peak-to-peak inductor ripple current, FOSC is the switching frequency, L is the inductance value, V_{IN} is the input voltage, V_{OUT} is the output voltage, RESR is the equivalent series resistance value of the output capacitor, and the C_{OUT} is the output capacitor. When using the ceramic capacitors, the RESR can be ignored and the output ripple voltage Δ V_{OUT} is shown as:

$$\Delta V_{OUT} = \frac{\Delta I}{8 \times Fosc \times C_{OUT}}$$

When using tantalum or electrolytic capacitors, typically 90% of the output voltage ripple is contributed by the ESR of output capacitors. the output ripple voltage Δ V_{OUT} can be estimated as:

$$\Delta V_{OUT} = \Delta I \times R_{ESR}$$

Output Inductor Selection

The output inductor is used for store energy and filter output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode. That will lower ripple current and results in lower output ripple voltage. A good rule for determining the inductance is set the peak-to-peak inductor ripple current Δ I almost equal to 30% of the maximum load current. Then the minimum inductance can be calculated with the following equation:

$$\Delta I = 0.3 \times I_{OUT}(max)$$

$$L \geq (V_{IN} - V_{OUT}) \times \left(\frac{V_{OUT}}{Fosc \times \Delta I \times V_{IN}}\right)$$

Where V_{IN} is the maximum input voltage.

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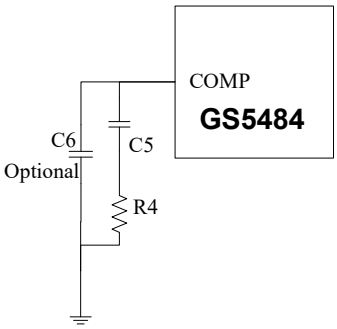
Compensation Components Selection



Selecting the appropriate compensation value by following procedure:
1. Calculate the R4 value with the following equation:

$$R4 < \frac{2\pi \times C_{OUT} \times 0.1 \times Fosc \times V_{OUT}}{G_{EA} \times Gcs \times V_{REF}}$$

where G_{EA} is the error amplifier voltage gain, and G_{CS} is the current sense gain.

2. Calculate the C5 value with the following equation:

$$C5 > \frac{4}{2\pi \times R4 \times 0.1 \times Fosc}$$

3. If the COUT ESR zero is less than half of the switching frequency, use C6 to cancel the ESR zero:

$$C6 = \frac{C_{OUT} \times R_{ESR}}{R4}$$

Boot-Strap Capacitor Selection

A 10nF ceramic capacitor must be connected between the BS pin to SW pin for proper operation.
It is recommended to use a ceramic capacitor

PCB Layout Recommendation

The device's performance and stability is dramatically affected by PCB layout. It is recommended to follow these general guidelines show bellow:

1. Place the input capacitors, output capacitors as close to the device as possible. Trace to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{IN} bypass capacitors close to the V_{IN} pin.
3. Place feedback resistors close to the FB pin.
4. Place compensation components close to the COMP pin.
5. Keep the sensitive signal (FB, COMP) away from the switching signal (SW).
6. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connects to the exposed pad should be maximized to improve thermal performance.
7. Multi-layer PCB design is recommended.

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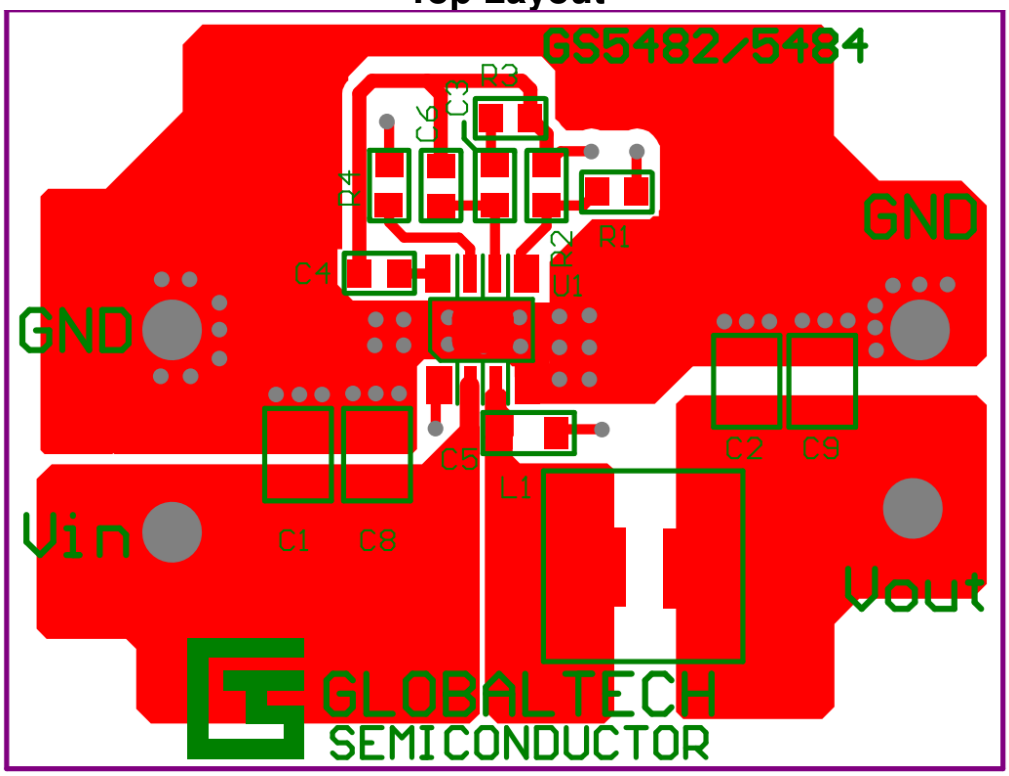
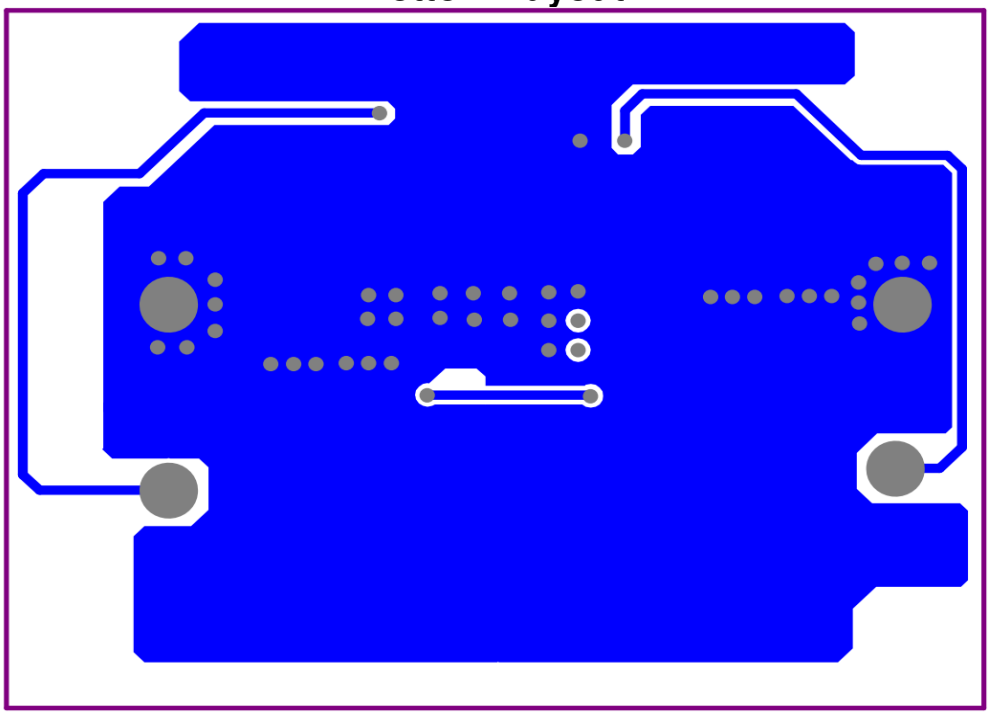
Top Layout



Bottom Layout



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